databook

SGS ATES

COS/MOS
B-SERIES
DEVICES
1st EDITION
ISSUED
JULY 1978

INTRODUCTION

This databook contains data sheets on the SGS-ATES range of COS/MOS B-series integrated circuits. The information on each product, in accordance with EIA/JEDEC specifications, has been specially presented in order that the performance of the product can be readily evaluated within any required equipment design.
In addition general considerations that should be taken into account in the operation and application of COS/MOS integrated circuits are described and selection guides are included to simplify the task of choosing the best combination of circuits for a system.
The databook also contains the results of the Reliability studies and of the improvements made by SGS-ATES to its COS/MOS family.
Information on SGS-ATES COS/MOS 4000A series and 4700A proprietary series has been published on the SGS-ATES PROFESSIONAL SEMICONDUCTOR DATABOOK 3.

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SGS-ATES 4000B SERIES INFORMATION

The new SGS-ATES COS/MOS **HCC/HCF 4000B** series meets the industry standardized specifications co-ordinated by EIA/JEDEC Solid State Products Council.
The official JEDEC specifications for static parameters are primarily applicable to gates, inverters, high current (inverting) drivers and devices with Medium Scale Integration.
Special types such as analog switches, multiplexers and multivibrators do not have the same input-output standards as the B series specifications but are still given with a B suffix because they satisfy the remaining JEDEC specifications.

SGS-ATES **HCC/HCF 4000B** types have the following Absolute Maximum Ratings:

Symbol	Description	Limits
V_{DD}	Supply voltage	-0.5 to 20 V
V_i	Input voltage	-0.5 to V_{DD} +0.5 V
I_i	DC input current (any input)	± 10 mA
P_{tot}	Total power dissipation (per package)	200 mW
	Dissipation per output transistor for T_{op}= full package temp. range	100 mW
T_{op}	Operating temperature for **HCC** types	-55 to 125 °C
	for **HCF** types	-40 to 85 °C
T_{stg}	Storage temperature	-65 to 150 °C

The Recommended Operating Conditions are specified as follows:

Symbol	Description	Limits
V_{DD}	Supply voltage	3 to 18 V
V_i	Input voltage	0 to V_{DD} V
T_{op}	Operating temperature for **HCC** types	-55 to 125 °C
	for **HCF** types	-40 to 85 °C

If these ratings are compared with the corresponding JEDEC values shown in table II and III it can be seen that the SGS-ATES **HCC/HCF 4000B** devices have much better limits than those of the JEDEC specifications.
The static electrical characteristics of the **HCC/HCF 4000B** series, excluding special devices such as analog switches, multiplexers, drivers, etc. are shown in table I.
The SGS-ATES **HCC/HCF 4000B** family has the quiescent leakage current (I_L) specified at 5, 10, 15, 20 V and the other static electrical characteristics at 5, 10, 15 V for both extended and intermediate temperature ranges.

HCC/HCF 4000B series features

The principal features of the **HCC/HCF 4000B** series are as follows:

- 3-18V operating range
- Rationalised range of quiescent leakage current (I_L) specifications corresponding to gate, buffer and flip-flop, and Medium Scale Integration products.
- Maximum input leakage current (I_{IH}, I_{IL}) of ± 1 μA at V_{DD}= 18V with V_i= 0 to 18 V over the full temperature range.
- Input and output logic levels completely independent of temperature.
- Input voltage levels which define a very high DC noise immunity (45% V_{DD} typical).
- Noise margins of 1 V min at 5V V_{DD}
  2 V min at 10V V_{DD}
  2.5V min at 15V V_{DD}
- Low (400 ohm typical) and constant output impedance in both logical states giving fixed and equal output transition times.
- Output current capable of driving

  a) two low power TTL loads
  b) one low power Schottky TTL load
  c) two HLL loads

  over the rated temperature range.
- Output current and input threshold independent of the number of inputs paralleled together.
- Square transfer voltage characteristics.

General COS/MOS characteristics

The main advantages offered by COS/MOS devices over corresponding bipolar devices (DTL, LPS, TTL, ECL, HLL) are:

- very low quiescent power dissipation (typically 10 nW/gate, 10 μW/MSI)
- wide operating voltage range (3 to 18V)
- high input impedance (typically 10^{12} Ω)
- high DC noise immunity (typically 45% of supply voltage).

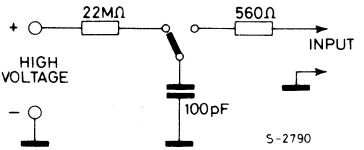
This digital family however has slower switching speeds than most bipolar families. For example the typical propagation times for COS/MOS and other logic families are:

	COS/MOS	ECL	LPS	TTL	DTL	HLL
Propagat. delay time (ns)	35	2	5	10	30	110

Moreover, due to the high input impedance of the MOS gates, COS/MOS devices require greater care in handling.
The normal gate oxide thickness is 800 to 1000 Å with a corresponding breakdown voltage between gate and substrate of 80 to 90V.
The electrostatic potential of the human body is much higher than this range, reaching 12 kV with a discharge capacity of approximately 100 pF. In fact an equivalent body discharge network is shown in fig. A.

SGS-ATES 4000B SERIES INFORMATION (continued)

Fig. A - Equivalent body discharge network



The characteristic values of electrostatic potential in an environment with relative humidity in the range 25% to 36% are as follow:

Source of electrostatic potential	Typical value (kV)	Maximum value (kV)
Person walking on a carpet	12	39
Person walking on vinyl tiles	4	13
Person working at a bench	0.5	3
16 pin DIP in a plastic box	3.5	12
16 pin DIP in plastic tubes used for shipping	0.5	3

Overvoltage protection networks are therefore used for the inputs of COS/MOS device.
The **HCC/HCF 4000B** devices use an improved protection network over that used in the **4000A** series. The level of protection for the **4000B** products has been raised to 4 kV , the previous solution for the **4000A** products protected the gate oxide against electrostatic discharges only up to approximately 1 kV. The following figures show the difference between the two input protection networks for a basic inverter:

Fig. B

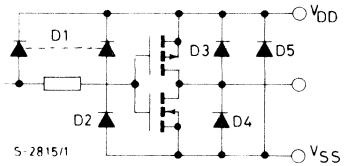
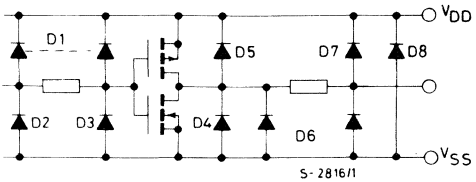


Fig. C



In COS/MOS as in Linear Integrated Circuits a "latch-up" phenomenon may appear. This is caused by an electrical pulse which, acting on an SCR structure of parasitic bipolar transistors inside COS/MOS devices (shown in fig. D), produces a low resistance path between supply voltage and ground that remains after the pulse has ceased leading rapidly to device destruction.

This phenomenon will occur either when V_{DD} is more than the maximum rating and approaches the breakdown voltage of the SCR structure or when the following conditions are verified:

a) the product of the gains of the two parasitic transistors is greater than or equal to unity;

b) the base-emitter junction of both transistors is forward biased;

c) supply voltage and input circuits are able to deliver a current equal to the holding current of the SCR (fig. E).

In particular, condition (b) may be caused by:

1) voltages induced through the oxide by based metallization;

2) lateral voltage drops between substrate and P-well due to photo current generated by radiation. These drops can forward bias the gate-cathode junction of the parasitic SCR.

This effect is particularly significant in buffers which are devices most subject to latch-up due to the combination of large geometry and low silicon resistivity.
For these reasons voltage transients or large output current surges occurring during operation near the maximum rating should be avoided.

Fig. D

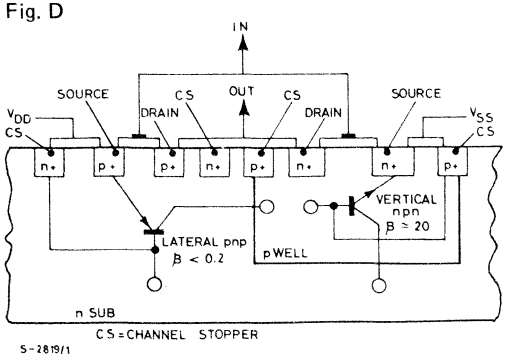
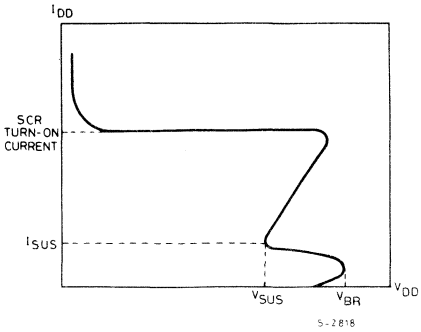


Fig. E



The B series devices are much better protected against latch-up than the A series because of their higher typical breakdown voltage:

Characteristic	A series	B series
V_{BR}	17 V	25 V
V_{SUS}	15 V	22 V
I_{SUS}	10 to 40 mA	50 to 100 mA

B series dynamic switching parameters

The dynamic electrical characteristics are specified at T_{amb}= 25°C under the following conditions:

- load capacitance (C_L) of 50 pF and load resistance (R_L) of 200 kΩ;
- input pulse amplitude equal to supply voltage (V_{DD});
- input rise and fall times of 20 ns;
- propagation delay times measured from 50% the point of the input voltage to the 50% point of the output voltage;
- transition times measured from 10% to 90% of the supply voltage (V_{DD}).

In some devices other time parameters are also specified:

a) Set up time
b) Hold time
c) Removal time
d) Tri-state disable delay times.

The figures below show the meaning of these parameters:

Fig. F

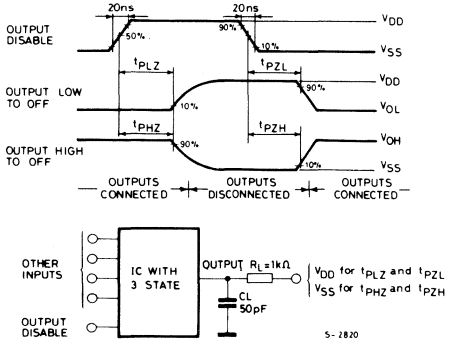
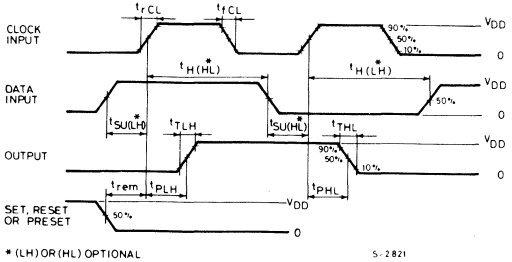


Fig. G



Comparison between B and UB devices

The **HCC/HCF 4000B** family also includes suffix UB products that only meet some of the B series electrical specifications.
These have logic outputs that are not buffered, and V_{IL} and V_{IH} that are specified as 20% V_{DD} and 80% V_{DD} respectively for V_{DD}= 5V and 10V and 17% V_{DD} and 83% V_{DD} respectively for V_{DD}= 15V.

The corresponding values of suffix B types are:

V_{IL}= 30% V_{DD}
V_{IH}= 70% V_{DD} for V_{DD}= 5V and 10V and V_{IL}= 27% V_{DD}
V_{IH}= 73% V_{DD} for V_{DD}= 15V

The other main differences between B and UB gates are summarized below:

Characteristic	Buffered	Unbuffered
Typical output impedance	Constant: 400 Ω (typ.) at V_{DD}= 5V	Variable: dependent on number of inputs paralleled together
Voltage transfer characteristic	Square and independent of the number of inputs tied together	Rounded (as A series) and shifted with different number of inputs paralleled together
Propagation delay	Moderate: 150 ns at V_{DD}= 5V 65 ns at V_{DD}= 10V 50 ns at V_{DD}= 15V	Fast: 60 ns at V_{DD}= 5V 30 ns at V_{DD}= 10V 25 ns at V_{DD}= 15V
AC gain	High and constant: ≃ 68 dB	Low and dependent on supply voltage: 28 dB at V_{DD}= 5V 23 dB at V_{DD}= 10V 18 dB at V_{DD}= 15V
AC band width	Low: 230 kHz at V_{DD}= 5V 280 kHz at V_{DD}= 10V 295 kHz at V_{DD}= 15V	High: 710 kHz at V_{DD}= 5V 885 kHz at V_{DD}= 10V 2800 kHz at V_{DD}= 15V
Input capacitance	Low: average 1 to 2 pF peak 2 to 4 pF	High: average 2 to 3 pF peak 5 to 10 pF
Noise margin	Excellent: 1V at V_{DD}= 5V 2V at V_{DD}= 10V 2.5V at V_{DD}= 15V	Good: 0.5V at V_{DD}= 5V 1V at V_{DD}= 10V 1V at V_{DD}= 15V
Output transition time	200 ns (typ.) at V_{DD}= 5V C_L = 50 pF	50 to 100 ns at V_{DD}= 5V C_L = 50 pF

If B and UB gates are presented with slow transition time signals the behaviour of the two types differs. In fact, because of high AC gain of B devices (obtained with the two extra inverters) the outputs tend to develop a few cycles of oscillation between V_{DD} and V_{SS} when input rise or fall time is more than 1 ms at V_{DD}= 5V and AC noise is reduced to 2 – 3 mV within the B device bandwidth.
The unbuffered gates (which have less gain) tend not to oscillate with the same input ramp unless a noise voltage of 200 to 300 mV is present within the device bandwidth.

GENERAL OPERATING AND HANDLING INSTRUCTIONS

Power source rules

1) Referring to standard input network protection of fig. B, when separate power supplies are used for V_{DD} and for the device inputs, the V_{DD} supply should always be turned on before the input signal source and the input signal should be turned off before the V_{DD} supply is turned off.
This rule will prevent the D1 input protection diode from overdissipation and possible damage when the device power supply is grounded.
When the device power supply is an open circuit, violation of this rule can result in undesired circuit operation although device damage may not result; AC inputs can be rectified by D1 input diode to act as a power supply.

2) The steady power-supply operating voltage should be kept within the recommended operating conditions and always below the maximum ratings.

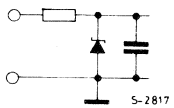
3) The power-supply polarity for COS/MOS circuits should not be reversed. The positive (V_{DD}) terminal should never be more than 0.5V negative with respect to the negative (V_{SS}) terminal (V_{DD}-$V_{SS} > -0.5V$). Reversal of polarities will forward-bias and short the structural and protection diode between V_{DD} and V_{SS}.

4) Power-source current capability should be limited to the minimum value which will assure good logic operation.

5) Large values of resistors in series with V_{DD} or V_{SS} should be avoided; transient turn-on of input protection diodes can result from drops across such resistors during switching.

A good practice is to use a zener protection diode in parallel with the power bus as shown in fig. H below.
The zener value should be above the expected maximum regulation excursion, but should not exceed the maximum supply voltage.
A current limiting resistor is included if the supply impedance is lower than the zener power dissipation rating allow for a given zener voltage.
The shunt capacitor value is chosen to supply required peak current switching transients.

Fig. H



Input signal rules

1) Signals should not be applied to the inputs while the device power supply is off unless the input current is limited to a steady-state value of less than 10 mA. Input-signal interfaces that swing the allowable 0.5V above V_{DD} or below V_{SS} should be current-limited to 10 mA or less.
Whenever the possibility of exceeding 10 mA of input current exists, a resistor in series with the input must be used. The value of this resistor can be as high as 10 kΩ without affecting static electrical characteristics. However, speed will be reduced because of the added RC time constant.
Particular attention should be given to long input-signal lines where high inductance can increase the likelihood of large-signal pickup in noisy environments. In these cases, series resistance with shunt capacitance at the IC input terminals is recommended. The shunt capacitance should be made as large as possible consistent with the system speed requirements.

2) All COS/MOS inputs should be terminated. When COS/MOS inputs are wired to edge card connectors with COS/MOS drive coming from another PC board, a shunt resistor should be connected to V_{DD} or V_{SS}.

3) When COS/MOS circuits are driven by TTL logic a pull-up resistor should be connected from the COS/MOS inputs to 5V.

4) Input signals should be maintained within the recommended input signal swing range.

5) Input rise and fall times for clocked devices must not exceed 15 μs in order to avoid high consumption, false triggering, etc. With slower inputs a Schmitt trigger must be employed.

Output rules

1) The power dissipation in a COS/MOS package should not exceed the rated value for the ambient temperature specified. The actual dissipation should be calculated when (a) shorting outputs directly to V_{DD} or V_{SS}, (b) driving low-impedance loads, or (c) directly driving the base of PNP or NPN bipolar transistors.

2) Output short circuits often result from testing errors or improper board assembly. Shorts on buffer outputs on power supplies greater than 5V can damage COS/MOS devices.

3) COS/MOS, like active pull-up TTL, cannot be connected in the "wire-OR" configuration because an "on" PMOS and an "on" NMOS transistor could be directly shorted across the power-supply rails. For applications with wire OR configurations it is necessary to use devices with tri-state logic outputs.

4) Paralleling gates is recommended only when the gates are within the same IC package.

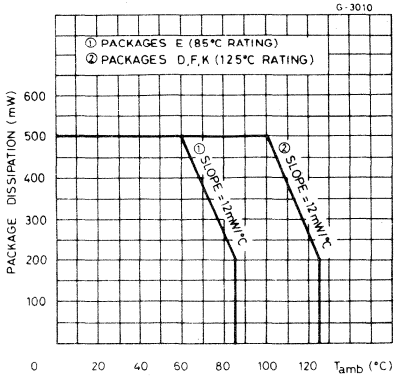
5) Output loads should return to a voltage within the supply-voltage range (V_{DD} to V_{SS}).

6) Large capacitive loads (greater than 5000 pF) on COS/MOS buffers or high-current drivers act like short circuits and may over-dissipate output transistors.

7) Output transistors may be over-dissipated by operating buffers as linear amplifiers or using these types as one-shot or astable multivibrators.

8) Shorting of output to V_{SS} or V_{DD} can cause the device power dissipation to exceed the safe value of 500 mW as shown in fig. I.
This is possible with supply voltage higher than 5V.
For cases in which a short circuited load is driven directly (base of PNP or NPN bipolar transistor) the requirements for gate operation must be determined by consulting the published data. Note that a individual output transistor dissipation must be limited to 100 mW.

Fig. I - Standard COS/MOS thermal derating chart



GENERAL OPERATING AND HANDLING INSTRUCTIONS (continued)

Noise Immunity and Noise Margin

DC Noise Immunity

The V_{IL} and V_{IH} characteristics define the maximum tolerable noise voltages at an input terminal when input signals are within 50 mV of supply lines.

Noise Margin

The noise margin voltage is the maximum voltage that can be added, at an input voltage $V_i = V_{OL}$ or V_{OH} of the preceding stage without upsetting the logic or causing the output to exceed the output voltage V_o.
In practice, DC noise immunity is much more significant than noise margin because the COS/MOS outputs are normally within 50 mV of supply lines. Noise immunity increases if the input pulse width becomes less than the propagation delay of the circuit.
This condition is often described as AC noise immunity.

Handling rules

Since each user's manufacturing environment is different it is only possible to give some general notes for avoiding damage from electrostatic voltages:

a) handling equipment, trays, table tops and transport carts should be conductive;

b) metal parts of fixtures, tools, soldering irons and table tops should be grounded to a common point;

c) operators should use grounded (metal or conductive) plastic wrist straps with a 1 MΩ series resistor;

d) packages should not be removed from their conductive or antistatic carriers until required; this should only be done by a grounded operator. Devices removed should be placed in a conductive tray;

e) all tests should be performed by a grounded operator and after completion of test, devices should be reinserted in conductive carriers;

f) the printed circuit boards should have shorting bars installed prior to assembly (soldering). When possible COS/MOS IC's should be the last component installed on PC boards.

Table I - STATIC ELECTRICAL CHARACTERISTICS (SGS-ATES 4000B and UB)

Parameter		Test conditions				Values						Unit
		V_i (V)	V_o (V)	$\|I_o\|$ (μA)	V_{DD} (V)	T_{Low}		25°C		T_{High}		
						Min.	Max.	Min.	Max.	Min.	Max.	
I_L (gates)					5		0.25		0.25		7.5	μA
					10		0.5		0.5		15	
					15		1		1		30	
					20		5		5		150	
I_L (buffer, FF)					5		1		1		30	μA
					10		2		2		60	
					15		4		4		120	
					20		20		20		600	
I_L (MSI)					5		5		5		150	μA
					10		10		10		300	
					15		20		20		600	
					20		100		100		3000	
V_{OH}		0/ 5		< 1	5	4.95		4.95		4.95		V
		0/10		< 1	10	9.95		9.95		9.95		
		0/15		< 1	15	14.95		14.95		14.95		
V_{OL}		5/0		< 1	5		0.05		0.05		0.05	V
		10/0		< 1	10		0.05		0.05		0.05	
		15/0		< 1	15		0.05		0.05		0.05	
V_{IH} (B series)			0.5/4.5	< 1	5	3.5		3.5		3.5		V
			1/9	< 1	10	7		7		7		
			1.5/13.5	< 1	15	11		11		11		
V_{IL} (B series)			4.5/0.5	< 1	5		1.5		1.5		1.5	V
			9/1	< 1	10		3		3		3	
			13.5/1.5	< 1	15		4		4		4	
V_{IH} (UB series)			0.5/4.5	< 1	5	4		4		4		V
			1/9	< 1	10	8		8		8		
			2/13	< 1	15	12		12		12		
V_{IL} (UB series)			4.5/0.5	< 1	5		1		1		1	V
			9/1	< 1	10		2		2		2	
			13/2	< 1	15		3		3		3	
I_{OH}	HCC	0/ 5	2.5		5	-2		-1.6		-1.15		mA
		0/ 5	4.6		5	-0.64		-0.51		-0.36		
		0/10	9.5		10	-1.6		-1.3		-0.9		
		0/15	13.5		15	-4.2		-3.4		-2.4		
	HCF	0/ 5	2.5		5	-1.8		-1.6		-1.3		mA
		0/ 5	4.6		5	-0.61		-0.51		-0.42		
		0/10	9.5		10	-1.5		-1.3		-1.1		
		0/15	13.5		15	-4		-3.4		-2.8		
I_{OL}	HCC	0/ 5	0.4		5	0.64		0.51		0.36		mA
		0/10	0.5		10	1.6		1.3		0.9		
		0/15	1.5		15	4.2		3.4		2.4		
	HCF	0/ 5	0.4		5	0.61		0.51		0.42		mA
		0/10	0.5		10	1.5		1.3		1.1		
		0/15	1.5		15	4		3.4		2.8		
I_i		0/18			18		± 0.1		± 0,1		± 1	μA
I_o -3 state		0/18	0/18		18		+ 2		+ 2		+ 20	μA
C_i									7.5			pF
$C_{i(UB)}$									22.5			pF

STANDARD JEDEC SPECIFICATIONS

Table II - ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Limits
V_{DD}	Supply voltage	-0.5 to 18 V
V_i	Input voltage	-0.5 to V_{DD} +0.5 V
I_i	DC input current (any input)	± 10 mA
T_{st}	Storage temperature range	-65 to 150 °C

Table III - RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Limits
V_{DD}	Supply voltage	3 to 15 V
V_i	Input voltage	0 to V_{DD} V
T_{op}	Operating temperature for extended range devices	-55 to 125 °C
	for intermediate range devices	-40 to 85 °C

Table IV - STATIC ELECTRICAL JEDEC CHARACTERISTICS

Parameter		Test conditions				Values						Unit
		V_i (V)	V_o (V)	$\|I_o\|$ (μA)	V_{DD} (V)	T_{Low}		25°C		T_{High}		
						Min.	Max.	Min.	Max.	Min.	Max.	
I_L (gates)	HCC				5		0,25		0.25		7,5	
					10		0.5		0.5		15	μA
					15		1		1		30	
	HCF				5		1		1		7,5	
					10		2		2		15	μA
					15		4		4		30	
I_L (buffer FF)	HCC				5		4		4		30	
					10		8		8		60	μA
					15		16		16		120	
	HCF				5		4		4		30	
					10		8		8		60	μA
					15		16		16		120	
I_L (MSI)	HCC				5		5		5		150	
					10		10		10		300	μA
					15		20		20		600	
	HCF				5		20		20		150	
					10		40		40		300	μA
					15		80		80		600	
V_{OL}		0/ 5		< 1	5		0.05		0.05		0.05	
		0/10		< 1	10		0.05		0.05		0.05	V
		0/15		< 1	15		0.05		0.05		0.05	
V_{OH}		5/0		< 1	5	4.95		4.95		4.95		
		10/0		< 1	10	9.95		9.95		9.95		V
		15/0		< 1	15	14.95		14.95		14.95		
V_{IL}			0.5/4.5	< 1	5		1.5		1.5		1.5	
			1/9	< 1	10		3		3		3	V
			1.5/13.5	< 1	15		4		4		4	
V_{IH}			4.5/0.5	< 1	5	3.5		3.5		3.5		
			9/1	< 1	10	7		7		7		V
			13.5/1.5	< 1	15	11		11		11		
I_{OL}	HCC	0/ 5	0.4		5	0.64		0.51		0.36		
		0/10	0.5		10	1.6		1.3		0.9		mA
		0/15	1.5		15	4.2		3.4		2.4		
	HCF	0/ 5	0.4		5	0.52		0.44		0.36		
		0/10	0.5		10	1.3		1.1		0.9		mA
		0/15	1.5		15	3.6		3		2.4		
I_{OH}	HCC	0/ 5	4.6		5	-0.25		-0.2		-0.14		
		0/10	9.5		10	-0.62		-0.5		-0.35		mA
		0/15	13.5		15	-1.8		-1.5		-1.1		
	HCF	0/ 5	4.6		5	-0.2		-0.16		-0.12		
		0/10	9.5		10	-0.5		-0.4		-0.3		mA
		0/15	13.5		15	-1.4		-1.2		-1.0		
I_i	HCC	0/15			15		± 0.1		± 0.1		± 1	μA
	HCF	0/15			15		± 0.3		± 0.3		± 1	μA
C_i									7.5			pF

DATA-SHEETS

COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

NOR GATES: DUAL 3 INPUT PLUS INVERTER HCC/HCF 4000B
QUAD 2 INPUT HCC/HCF 4001B
DUAL 4 INPUT HCC/HCF 4002B
TRIPLE 3 INPUT HCC/HCF 4025B

- PROPAGATION DELAY TIME = 60 ns (TYP.) AT C_L = 50 pF, V_{DD} = 10V
- BUFFERED INPUTS AND OUTPUTS
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMP. RANGE)
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4000B**, **HCC 4001B**, **HCC 4002B** and **HCC 4025B** (extended temperature range) and **HCF 4000B**, **HCF 4001B**, **HCF 4002B** and **HCF 4025B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package, and ceramic flat package. The **HCC/HCF 4000B**, **HCC/HCF 4001B**, **HCC/HCF 4002B** and **HCC/HCF 4025B** NOR gates provide the system designer with direct implementation of the NOR function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

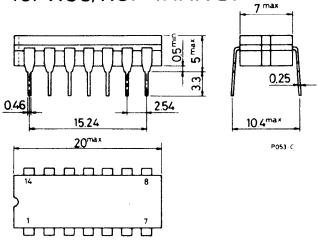
ORDERING NUMBERS:

HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

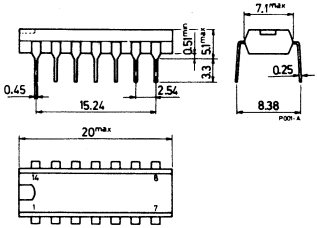
HCC/HCF 4000B
HCC/HCF 4001 B
HCC/HCF 4002B
HCC/HCF 4025B

MECHANICAL DATA (dimensions in mm)

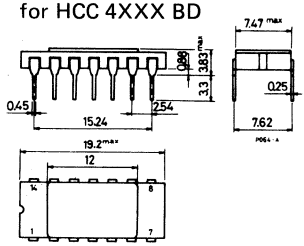
Dual in-line ceramic package
for HCC/HCF 4XXX BF



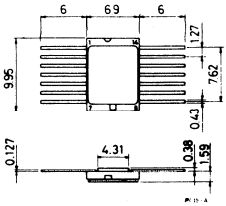
Dual in-line plastic package
for HCF 4XXX BE



Dual in-line ceramic package
for HCC 4XXX BD

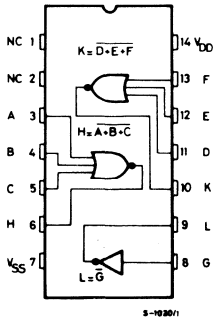


Ceramic flat package
for HCC 4XXX BK

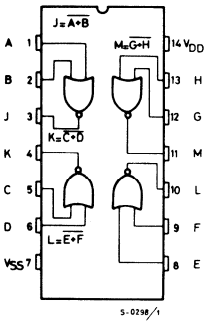


CONNECTION DIAGRAMS

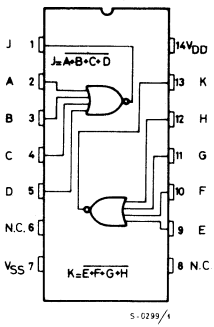
for **4000B**



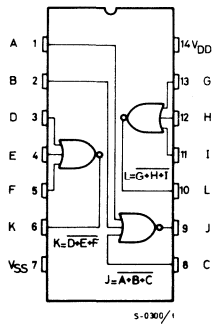
for **4001B**



for **4002B**



for **4025B**

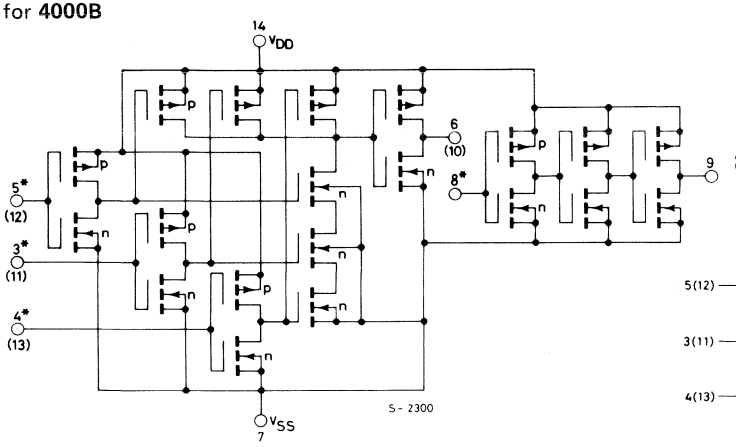


RECOMMENDED OPERATING CONDITIONS

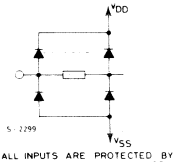
V_{DD}	Supply voltage	3 to 18 V
V_I	Input voltage	0 to V_{DD} V
T_{op}	Operating temperature: for **HCC** types	-55 to 125 °C
	for **HCF** types	-40 to 85 °C

SCHEMATIC AND LOGIC DIAGRAMS

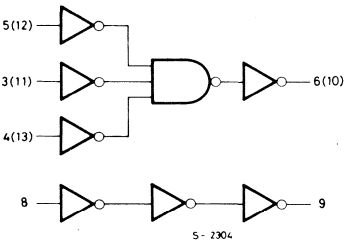
for **4000B**



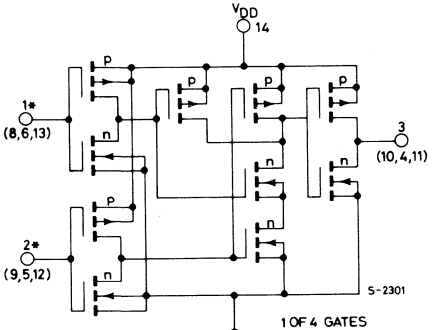
INVERTER AND 1 OF 2 GATES (NUMBERS IN PARENTHESES ARE THERMINAL NUMBERS FOR SECOND GATE)



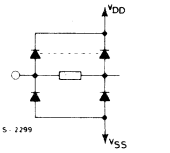
ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK



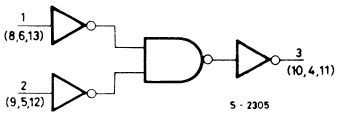
for **4001B**



1 OF 4 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

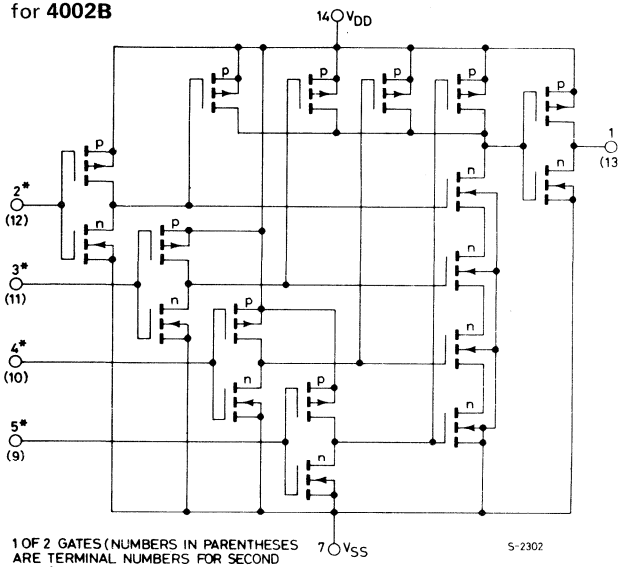


ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

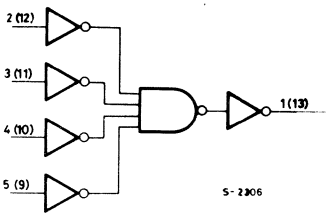


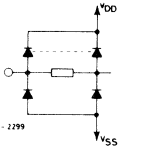
SCHEMATIC AND LOGIC DIAGRAMS (continued)

for **4002B**



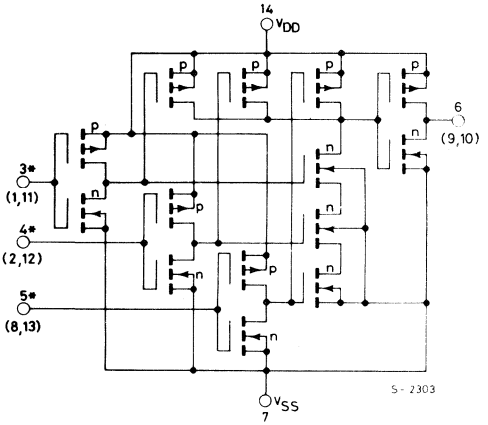
1 OF 2 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR SECOND GATE)



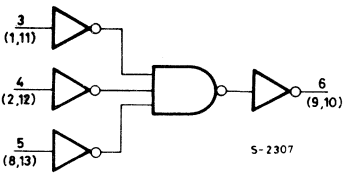


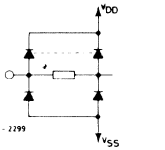
ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

for **4025B**



INVERTER AND 1 OF 3 GATES (NUMBERS IN PARENTHESES ARE THERMINAL NUMBERS FOR SECOND GATE)





ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

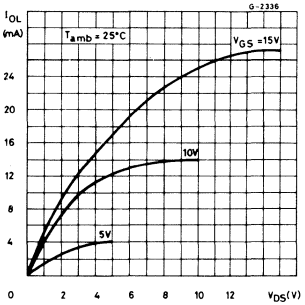
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				2/13	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13/2	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		±0.1		±10^{-5}	±0.1		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

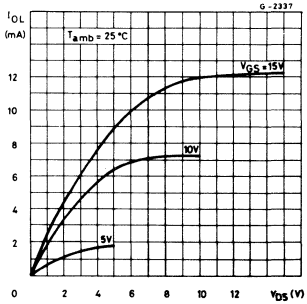
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH} Propagation delay time		5		125	250	ns
		10		60	120	
		15		45	90	
t_{THL}, t_{TLH} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	

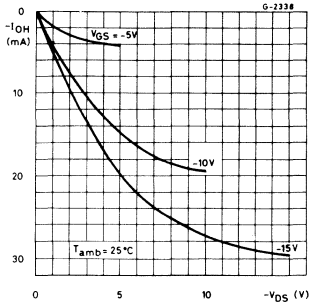
Typical output low (sink) current characteristics



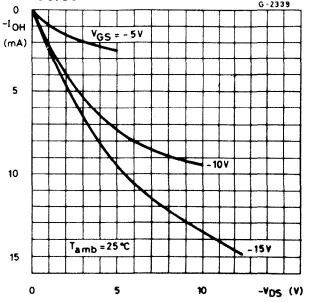
Minimum output low (sink) current characteristics



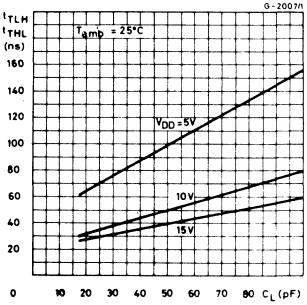
Typical output high (source) current characteristics



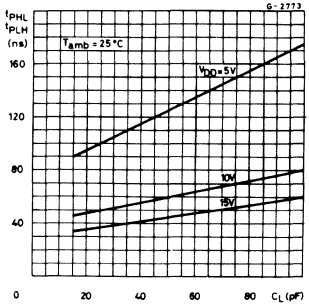
Minimum output high (source) current characteristics



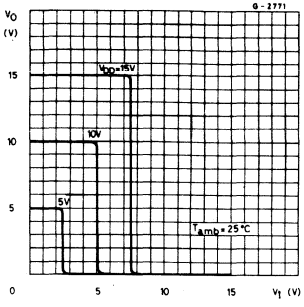
Typical transition time vs. load capacitance



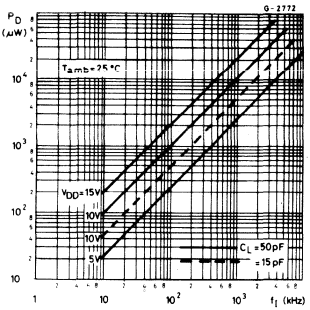
Typical propagation delay time vs. load capacitance



Typical voltage transfer characteristics as a function of temperature

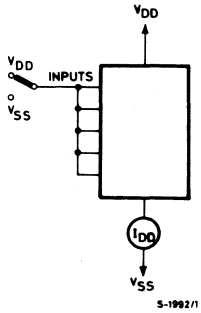


Typical power dissipation per gate vs. frequency

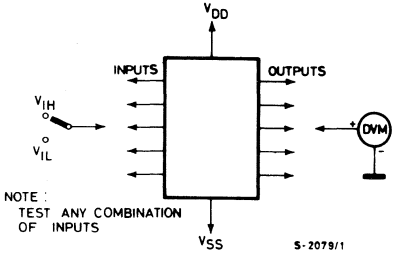


TEST CIRCUIT

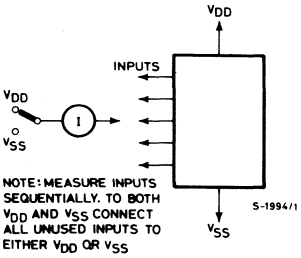
Quiescent device current



Input voltage



Input leakage current



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

18-STAGE STATIC SHIFT REGISTER

- PERMANENT REGISTER STORAGE WITH CLOCK LINE "HIGH" or "LOW" . . . . . NO INFORMATION RECIRCULATION REQUIRED
- FULLY STATIC OPERATION
- SHIFTING RATES UP TO 12 MHz @ 10V (TYP.)
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATING

The **HCC 4006B** (extended temperature range) and the **HCF 4006B** (standard temperature range), are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package. The types are comprised of 4 separate "shift register" sections; two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent "single rail" data path. A common clock signal is used for all stages. Data is shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 can be implemented using one **HCC/HCF 4006B** package. Longer shift register sections can be assembled by using more than one **HCC/HCF 4006B**. To facilitate cascading stages when clock rise and fall times are slow, an optional output (D_1 + 4') that is delayed one-half clock-cycle, is provided (see Truth Table for Output from pin 2).

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

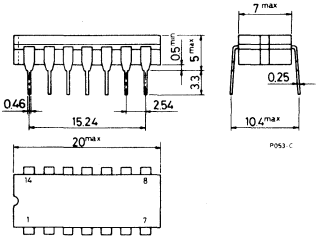
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

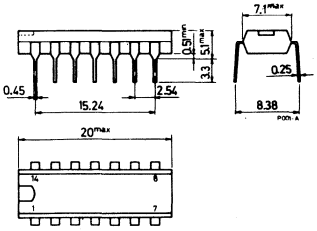
HCC 4006 BD	for dual in-line ceramic package
HCC 4006 BF	for dual in-line ceramic package, frit seal
HCC 4006 BK	for ceramic flat package
HCF 4006 BE	for dual in-line plastic package
HCF 4006 BF	for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

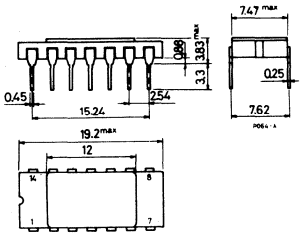
Dual in-line ceramic package
for HCC/HCF 4006 BF



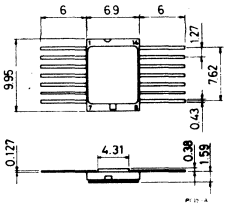
Dual in line plastic package
for HCF 4006 BE



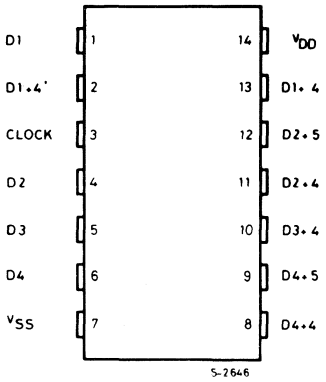
Dual in-line ceramic package
for HCC 4006 BD



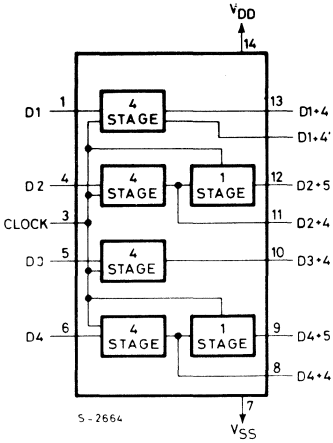
Ceramic flat package
for HCC 4006 BK



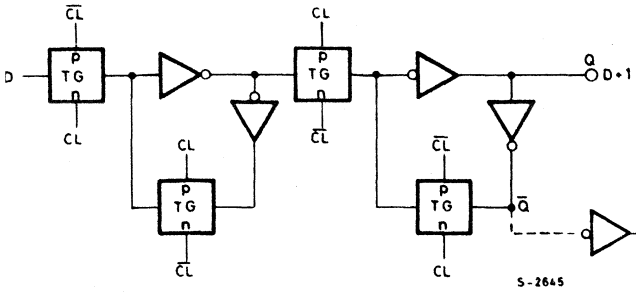
CONNECTION DIAGRAM

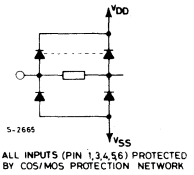


FUNCTIONAL DIAGRAM



LOGIC DIAGRAM AND TRUTH TABLE
(One register stage)





TRUTH TABLE FOR OUTPUT FROM PIN 2

$D_1 + 4$	CL▲	$D_1 + 4'$
0	⌐	0
1	⌐	1
X	⌐	NC

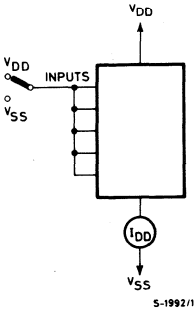
TRUTH TABLE FOR SHIFT REGISTER STAGE

D	CL▲	D + 1
0	⌐	0
1	⌐	1
X	⌐	NC

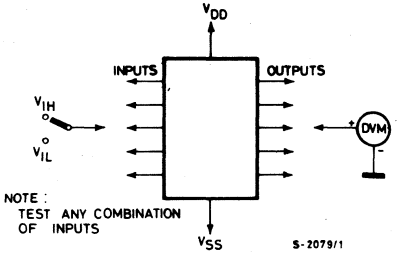
1 = = HIGH
0 = LOW
NC = NO CHANGE
X = DON'T CARE
▲ = LEVEL CHANGE

TESTS CIRCUITS

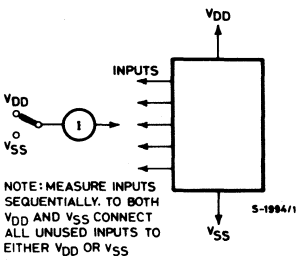
Quiescent device current



Input voltage



Input current



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5.	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		±0.1		±10^{-5}	±0.1		± 1	μA
C_i	Input capacitance			Any input						5	7.5			pF

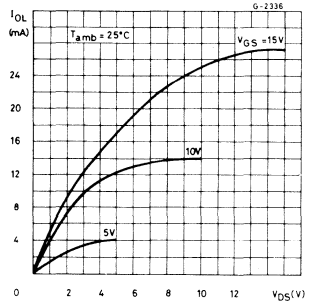
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

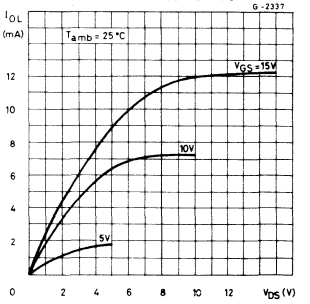
Parameter	Test conditions	Values			Unit
	V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time	5		200		ns
	10		100		
	15		80		
t_{THL}, t_{TLH} Transition time	5		100		ns
	10		50		
	15		40		
t_W Clock pulse width	5		100		ns
	10		45		
	15		30		
t_r, t_f Clock input rise or fall time*	5		15		μs
	10		15		
	15		15		
t_{setup} Data setup time	5		50		ns
	10		25		
	15		20		
f_{max} Maximum clock input frequency	5		5		MHz
	10		12		
	15		16		

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

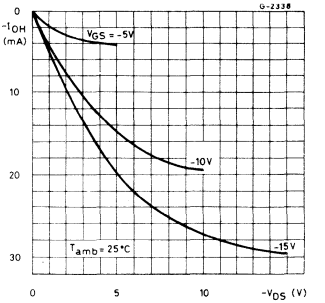
Typical output low (sink) current characteristics



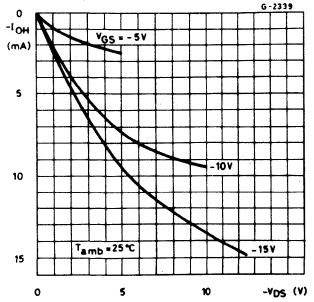
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics



Minimum output high (source) current characteristics)



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

DUAL COMPLEMENTARY PAIR PLUS INVERTER

- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- MEDIUM SPEED OPERATION t_{PHL}, t_{PLH} = 30 ns (TYP.) AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMP. RANGE)

The **HCC 4007UB** (extended temperature range) and **HCF 4007UB** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4007UB** types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in typical applications. More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

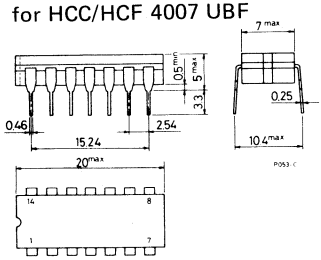
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

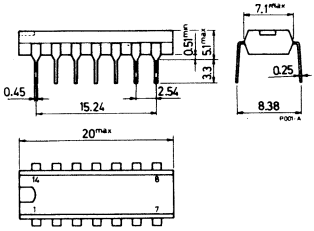
HCC 4007 UBD for dual in-line ceramic package
HCC 4007 UBF for dual in-line ceramic package, frit seal
HCC 4007 UBK for ceramic flat package
HCF 4007 UBE for dual in-line plastic package
HCF 4007 UBF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

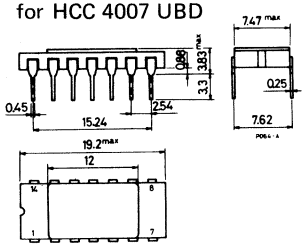
Dual in-line ceramic package
for HCC/HCF 4007 UBF



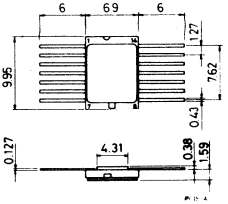
Dual in-line plastic package
for HCF 4007 UBE



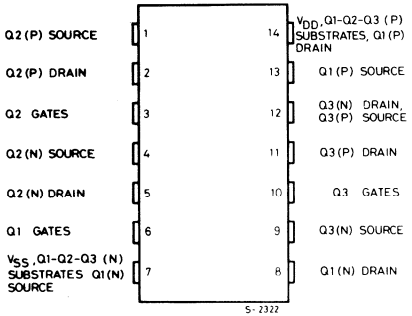
Dual in-line ceramic package
for HCC 4007 UBD



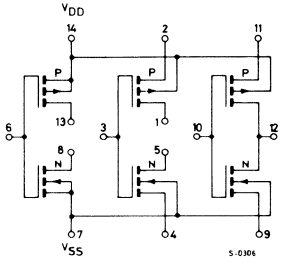
Ceramic flat package
for HCC 4007 UBK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

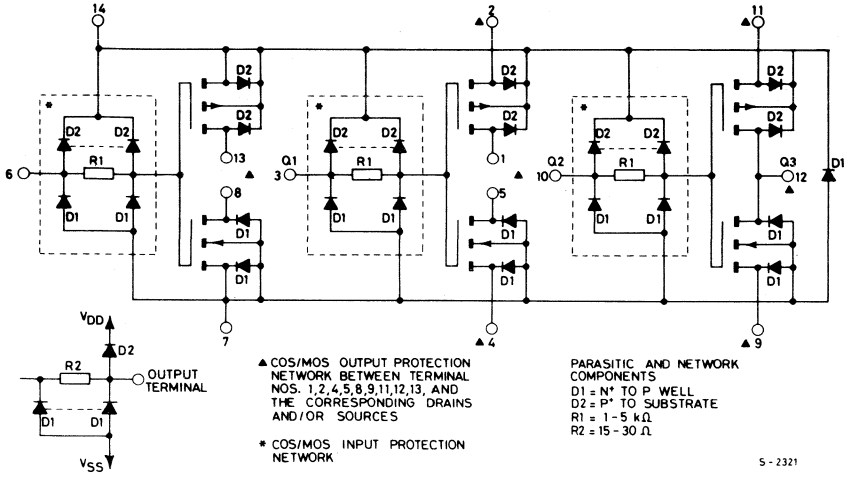


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

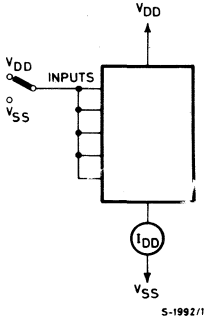
SCHEMATIC DIAGRAM

HCC/HCF 4007 UB showing input, output, and parasitic diodes

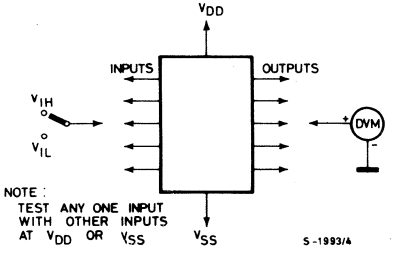


TEST CIRCUITS

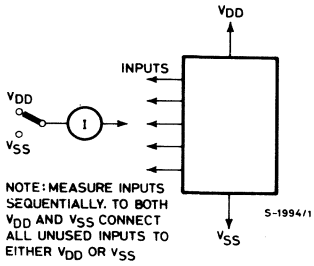
Quiescent device current



Input voltage



Input current



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

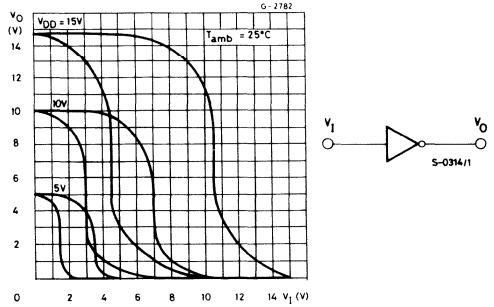
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	4		4			4		V
				1/9	< 1	10	8		8			8		
				2/13	< 1	15	12		12			12		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1			1		1	V
				9/1	< 1	10		2			2		2	
				13/2	< 1	15		3			3		3	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		±0.1		±10^{-5}	±0.1		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.

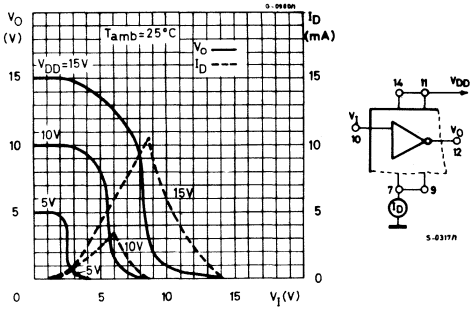
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
	V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time	5		55	110	ns
	10		30	60	
	15		25	50	
t_{TLH}, t_{THL} Transition time	5		100	200	ns
	10		50	100	
	15		40	80	

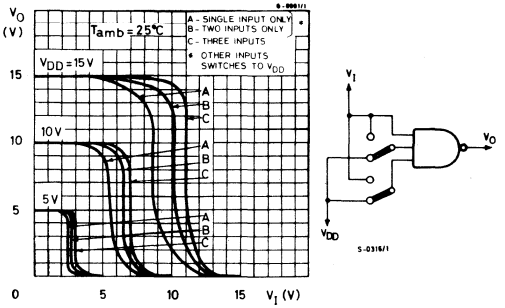
Minimum and maximum voltage-transfer characteristics for inverter and test circuit



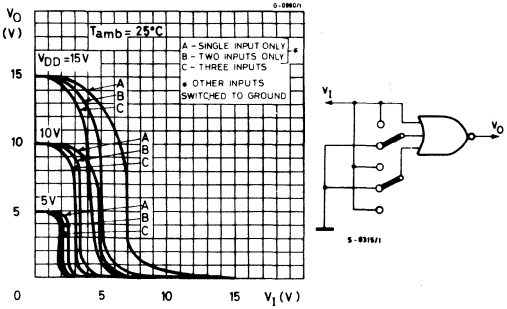
Typical current and voltage-transfer characteristics for inverter and test circuit



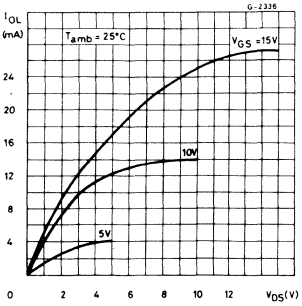
Typical voltage-transfer characteristics for NAND gate and test circuit



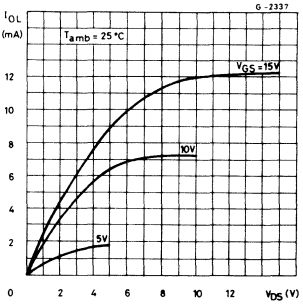
Typical voltage-transfer characteristics for NOR gate and test circuit



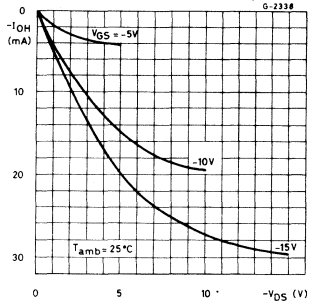
Typical output low (sink) current characteristics



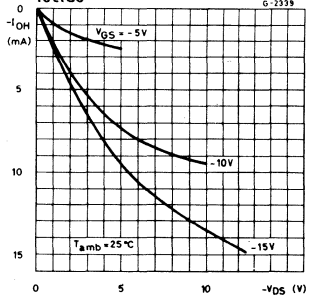
Minimum output low (sink) current characteristics



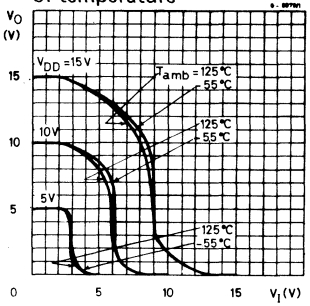
Typical output high (source) current characteristics



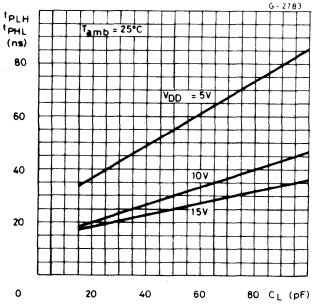
Minimum output high (source) current characteristics



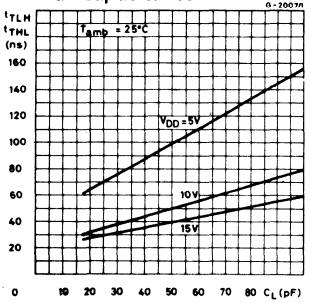
Typical voltage-transfer characteristics as a function of temperature



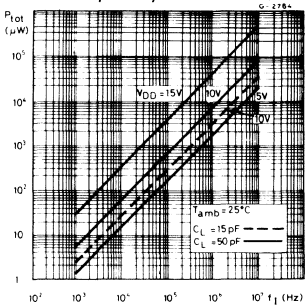
Typical propagation delay time vs. load capacitance



Typical transition time vs. load capacitance

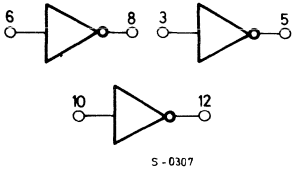


Typical dissipation per gate vs. frequency characteristics

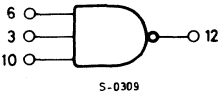


TYPICAL APPLICATIONS (sample COS/MOS logic circuit arrangements using type 4007 UB)

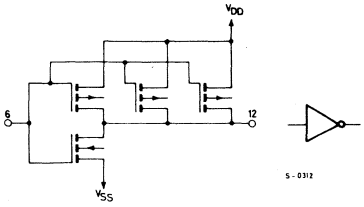
Triple inverters. (14, 2, 11); (8, 13); (1, 5); (4, 7, 9)



3-input NAND gate. (1, 12, 13); (2, 14, 11); (4, 8); (5, 9)

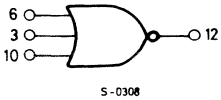


High source-current driver. (6, 3, 10); (13, 1, 12); (14, 2, 11); (7, 9)

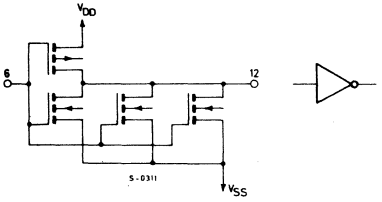


Dual bi-directional transmission gating. (1, 5, 12); (2, 9); (11, 4); (8, 13, 10); (6, 3)

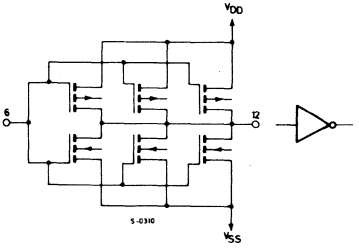
3-input NOR gate. (13, 2); (1, 11); (12, 5, 8); (7, 4, 9)

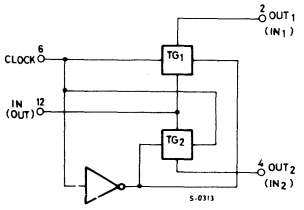


High sink-current driver. (6, 3, 10); (8, 5, 12); (11, 14); (7, 4, 9)



High sink-and source-current driver. (6, 3, 10); (14, 2, 11); (7, 4, 9); (13, 8, 1, 5, 12)





COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

4-BIT FULL ADDER WITH PARALLEL CARRY OUTPUT

- 4 SUM OUTPUTS PLUS PARALLEL LOOK-AHERD CARRY-OUTPUT
- HIGH-SPEED OPERATION-SUM IN-TO-SUM OUT 160 ns (TYP.): CARRY IN-TO-CARRY OUT 50 ns (TYP.) AT V_{DD}= 10V, C_L= 50 pF.
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATING

The **HCC 4008B** (extended temperature range) and **HCF 4008B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4008B** types consist of four full adder stages with fast look ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" to permit high-speed operation in arithmetic sections using several **HCC/HCF 4008B's**.
HCC/HCF 4008B inputs include the four sets of bits to be added, A_1 to A_4 and B_1 to B_4, in addition to the "Carry In" bit from a previous section. **HCC/HCF 4008B** outputs include the four sum bits, S_1 to S_4. In addition to the high speed "parallel-carry-out" which may be utilized at a succeeding **HCC/HCF 4008B** section.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

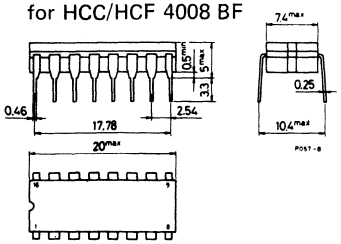
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

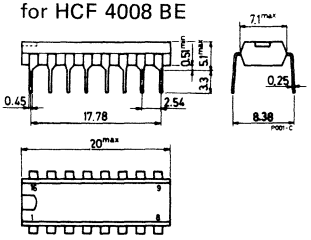
HCC 4008 BD for dual in-line ceramic package
HCC 4008 BF for dual in-line ceramic package, frit seal
HCC 4008 BK for ceramic flat package
HCF 4008 BE for dual in-line plastic package
HCF 4008 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

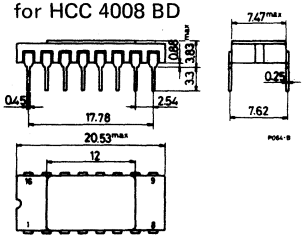
Daul in-line ceramic package
for HCC/HCF 4008 BF



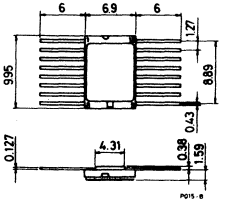
Dual in-line plastic package
for HCF 4008 BE



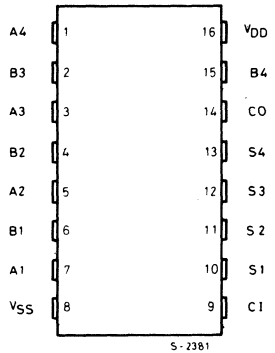
Dual in-line ceramic package
for HCC 4008 BD



Ceramic flat package
for HCC 4008 BK



CONNECTION DIAGRAM



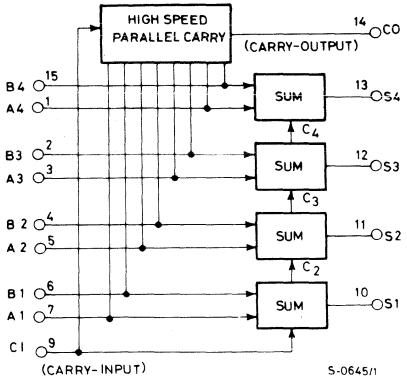
TRUTH TABLE

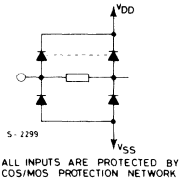
A_i	B_i	CI	CO	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

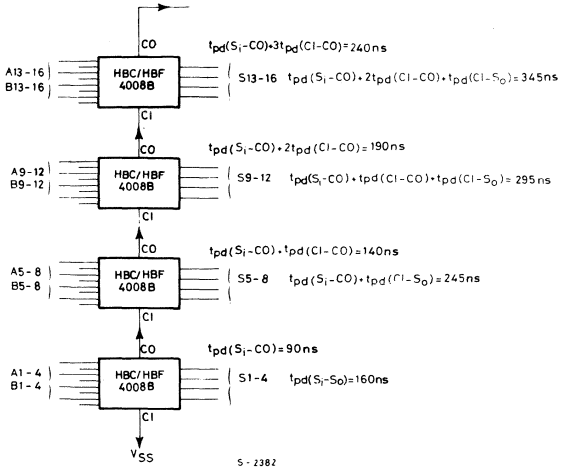
LOGIC DIAGRAM





TYPICAL APPLICATION

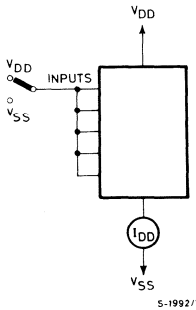
Speed characteristics of a 16-bit adder



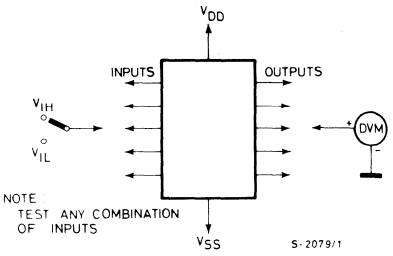
NOTES: All "A" and "B" input bits occur at t = 0
All sums settled at t = 345 ns.
C_L = 50 pF, T_{amb} = 25°C, V_{DD} - V_{SS} = 10V

TEST CIRCUITS

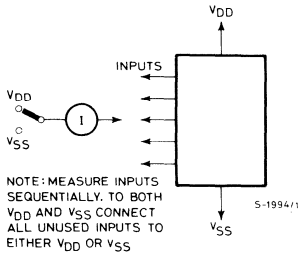
Quiescent device current



Input voltage



Input current



STATIC ELECTRICAL CHARACTERISTICS (under recommended operating conditions)

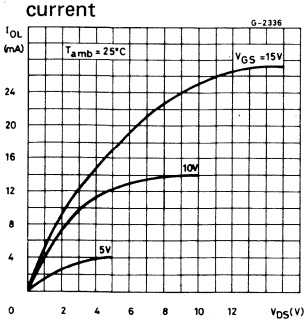
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		±1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

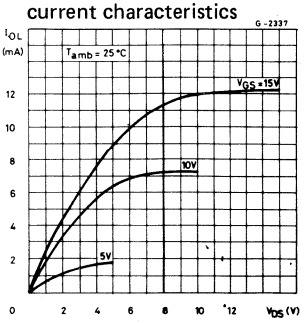
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values				Unit
			V_{DD}(V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time	Sum In to Sum Out		5		400	800	ns
			10		160	320	
			15		115	230	
	Carry In to Sum Out		5		370	740	
			10		155	310	
			15		115	230	
	Sum In to Carry Out		5		200	400	
			10		90	180	
			15		65	130	
	Carry In to Carry Out		5		100	200	
			10		50	100	
			15		40	80	
t_{THL}, t_{TLH} Transition time			5		100	200	ns
			10		50	100	
			15		40	80	

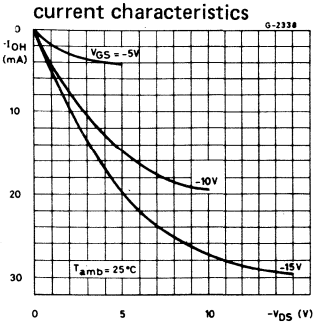
Typical output low (sink) current



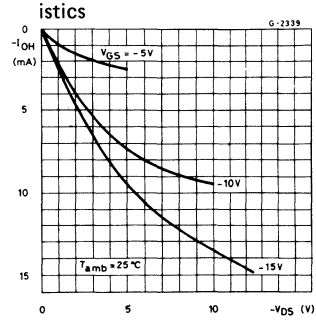
Minimum output low (sink) current characteristics



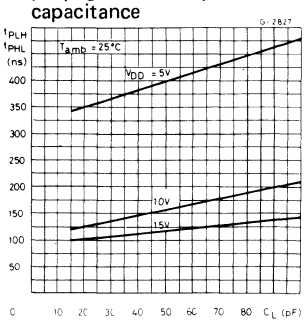
Typical output high (source) current characteristics



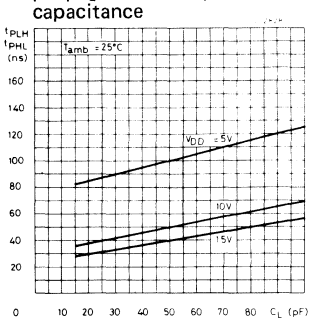
Minimum output high (source) current characteristics



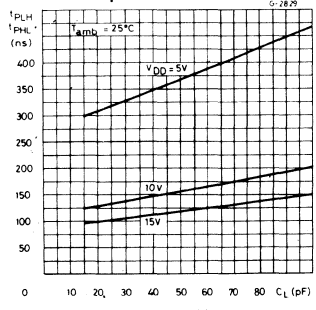
Typical sum-in to sum out propagation delay vs. load capacitance



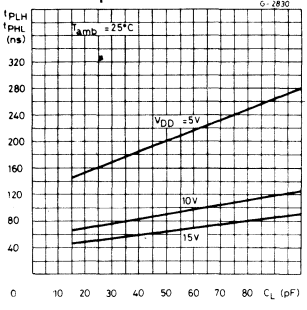
Typical carry-in to carry-out propagation delay vs. load capacitance



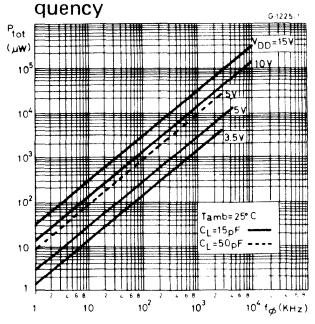
Typical carry-in to sum out propagation delay time vs. load capacitance



Typical sum-in to carry-out propagation delay time vs. load capacitance



Typical dynamic power dissipation/package vs. frequency



COS/MOS INTEGRATED CIRCUITS

HCC/HCF 4011 B
HCC/HCF 4012 B
HCC/HCF 4023B

PRELIMINARY DATA

NAND GATES: QUAD 2 INPUT HCC/HCF 4011B
DUAL 4 INPUT HCC/HCF 4012B
TRIPLE 3 INPUT HCC/HCF 4023B

- PROPAGATION DELAY TIME = 60 ns (TYP.) AT C_L = 50 pF, V_{DD} = 10V
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE TEMP. RANGE)
- 5V, 10V AND 15V PARAMETRIC RATINGS

The **HCC 4011B, HCC 4012B** and **HCC 4023B** (extended temperature range) and **HCF 4011B, HCF 4012B** and **HCF 4023B** (intermediate temperature range) are monolithic, integrated circuit,available in 14-lead dual in-line plastic or ceramic package, and ceramic flat package.
The **HCC/HCF 4011B, HCC/HCF 4012B** and **HCC/HCF 4023B** NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

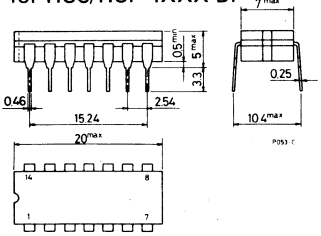
ORDERING NUMBERS:

HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

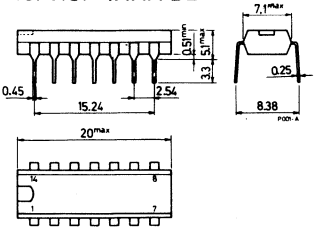
HCC/HCF 4011 B
HCC/HCF 4012 B
HCC/HCF 4023B

MECHANICAL DATA (dimensions in mm)

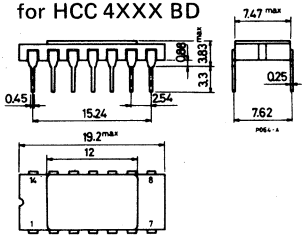
Dual in-line ceramic package
for HCC/HCF 4XXX BF



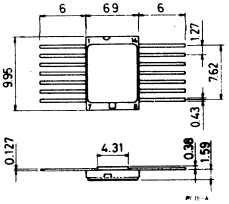
Dual in-line plastic package
for HCF 4XXX BE



Dual in-line ceramic package
for HCC 4XXX BD

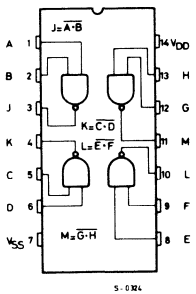


Ceramic flat package
for HCC 4XXX BK

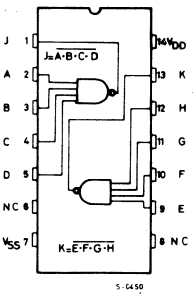


CONNECTION DIAGRAMS

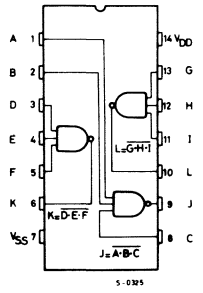
for **4011B**



for **4012B**



for **4023B**

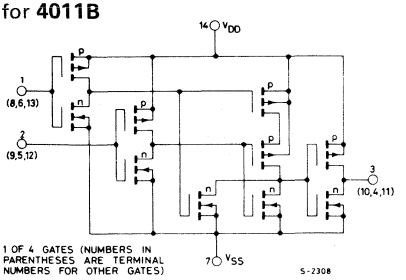


RECOMMENDED OPERATING CONDITIONS

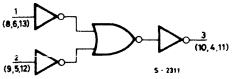
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

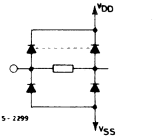
SCHEMATIC AND LOGIC DIAGRAMS

for **4011B**



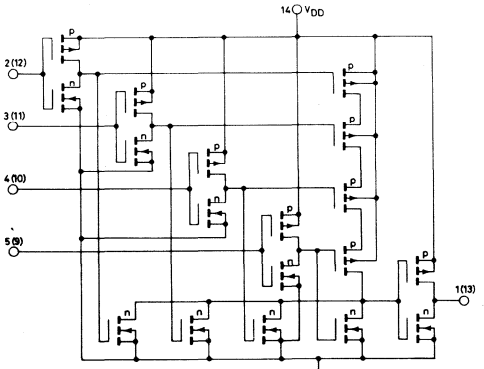
1 OF 4 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)



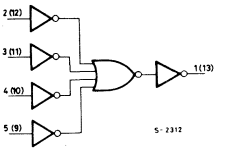


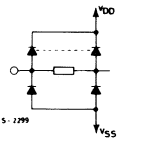
ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

for **4012B**



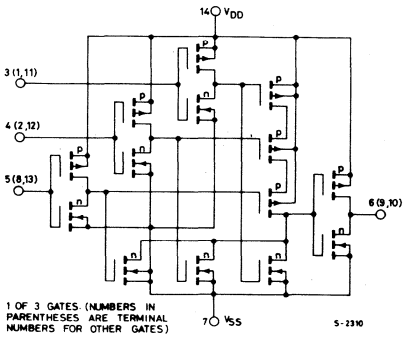
1 OF 2 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)



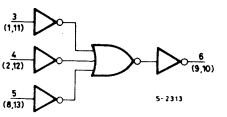


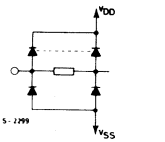
ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

for **4023B**



1 OF 3 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)





ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

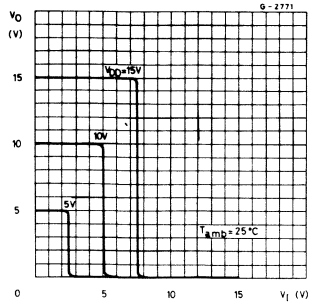
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				2/13	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13/2	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		±0.1		±10^{-5}	±0.1		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

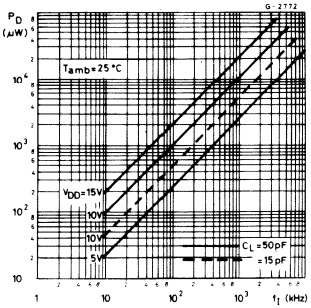
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
	V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time	5		125	250	ns
	10		60	120	
	15		45	90	
t_{THL}, t_{TLH} Transition time	5		100	200	ns
	10		50	100	
	15		40	80	

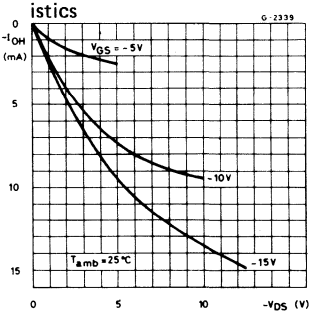
Typical voltage transfer characteristics



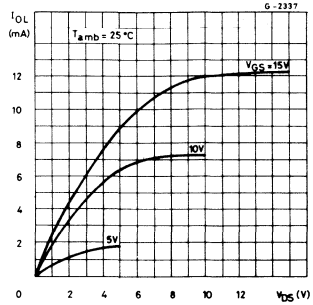
Typical power dissipation/ gate vs. frequency



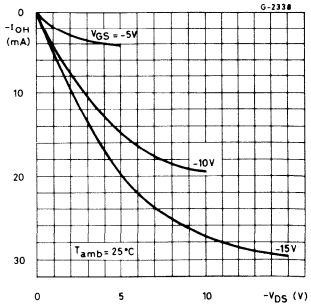
Minimum output high (source) current characteristics



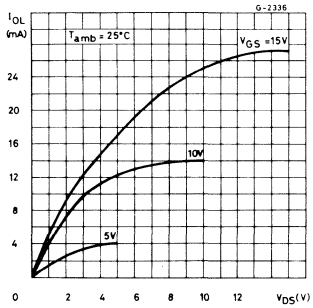
Minimum output low (sink) current characteristics



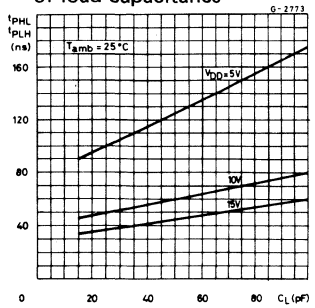
Typical output high (source) current characteristics



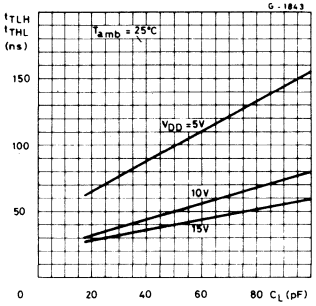
Typical output low (sink) current characteristics



Typical propagation delay time per gate as a function of load capacitance

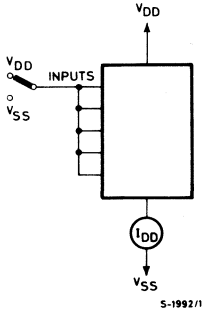


Typical transition time vs. load capacitance

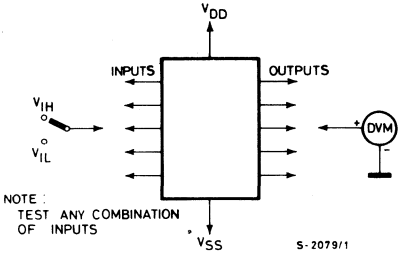


TEST CIRCUITS

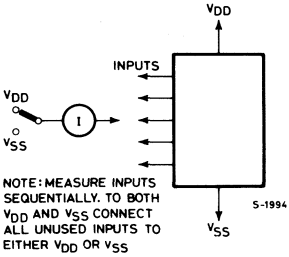
Quiescent device current



Noise immunity



Input leakage current



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

DUAL 'D' - TYPE FLIP-FLOP

- SET-RESET CAPABILITY
- STATIC FLIP-FLOP OPERATION - RETAINS STATE INDEFINITELY WITH CLOCK LEVEL EITHER "HIGH" OR "LOW"
- MEDIUM-SPEED OPERATION - 16 MHz (TYP.) CLOCK TOGGLE RATE AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT LEAKAGE OF 1 μA AT 18V (FULL PACKAGE TEMPERATURE RANGE)
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4013B** (extended temperature range) and **HCF 4013B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.

The **HCC/HCF 4013B** consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

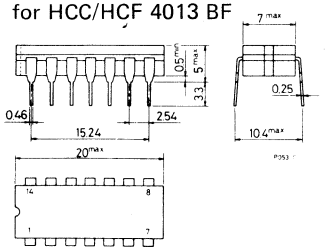
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

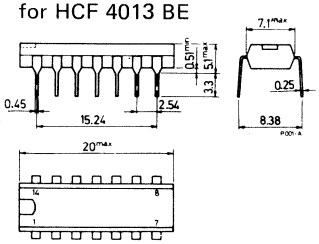
HCC 4013 BD	for dual in-line ceramic package
HCC 4013 BF	for dual in-line ceramic package, frit seal
HCC 4013 BK	for ceramic flat package
HCF 4013 BE	for dual in-line plastic package
HCF 4013 BF	for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

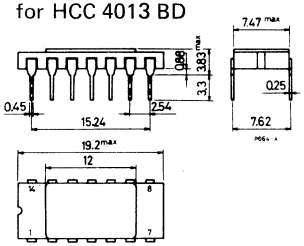
Dual in-line ceramic package for HCC/HCF 4013 BF



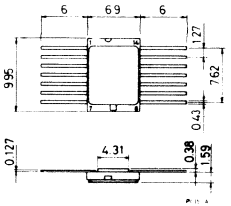
Dual in-line plastic package for HCF 4013 BE



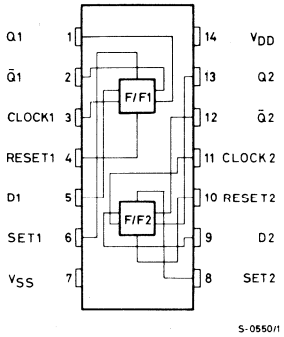
Dual in-line ceramic package for HCC 4013 BD



Ceramic flat package for HCC 4013 BK



CONNECTION DIAGRAM

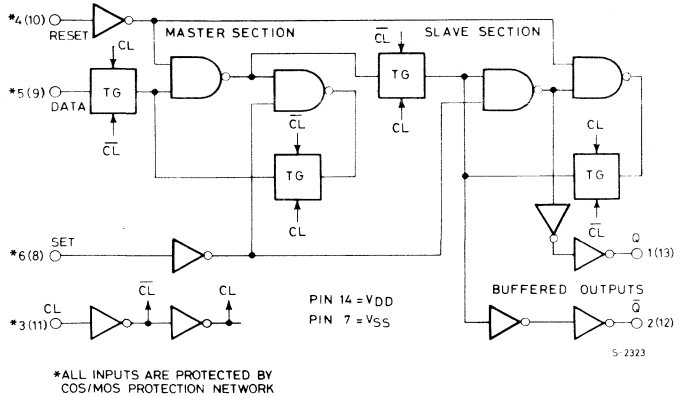


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM AND TRUTH TABLE

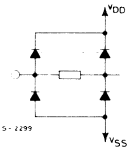
(one of two identical flip-flops)



*ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

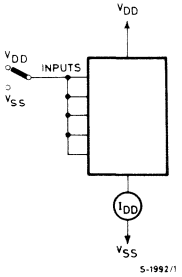
CL▲	D	R	S	Q	$\bar{Q}$	
⌒	0	0	0	0	1	
⌒	1	0	0	1	0	
⌣	X	0	0	Q	$\bar{Q}$	NO CHANGE
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

LOGIC 0=LOW ▲ =LEVEL CHANGE
LOGIC 1=HIGH X =DON'T CARE
N(N)=FF1/FF2 TERMINAL ASSIGNEMENT

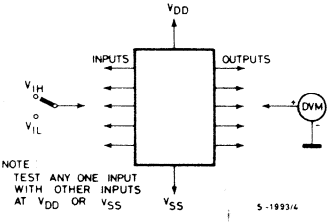


TEST CIRCUITS

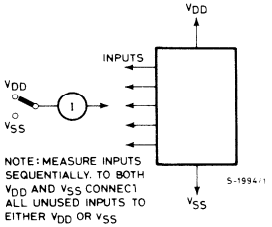
Quiescent device current



Noise immunity



Input leakage current



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				2/13	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13/2	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		±0.1		±10^{-5}	±0.1		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

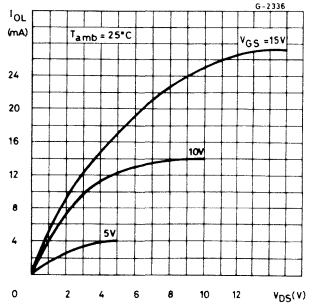
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time (clock to Q or $\overline{Q}$ outputs)		5		150	300	ns
			10		65	130	
			15		45	90	
t_{PLH}	Propagation delay time (Set to Q or Reset to $\overline{Q}$)		5		150	300	ns
			10		65	130	
			15		45	90	
t_{PHL}	Propagation delay time (Set to $\overline{Q}$ or Reset to Q)		5		200	400	ns
			10		85	170	
			15		60	120	
t_{THL}, t_{TLH}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
f_{CL}*	Maximum clock input frequency		5	3.5	7		MHz
			10	8	16		
			15	12	24		
t_W	Clock pulse width		5	140	70		ns
			10	60	30		
			15	40	20		
t_r,t_f**	Clock input rise or fall time		5			15	μs
			10			4	
			15			1	
t_W	Set or reset pulse width		5	180	90		ns
			10	80	40		
			15	50	25		
t_{setup}	Data setup time		5	40	20		ns
			10	20	10		
			15	15	7		

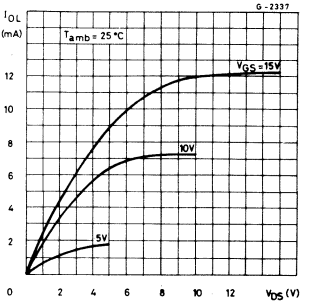
* Input t_r, t_f = 5 ns.

** If more than one unit is cascaded in a parallel clocked operation, t_r should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

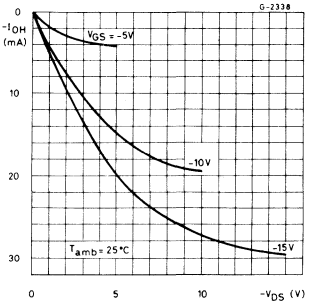
Typical output low (sink) current characteristics



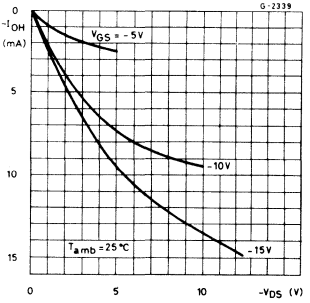
Minimum output low (sink) current characteristics



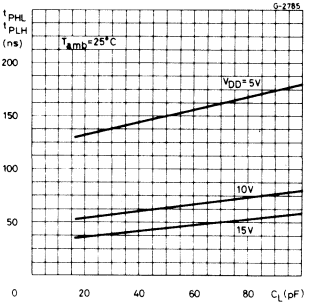
Typical output high (source) current characteristics



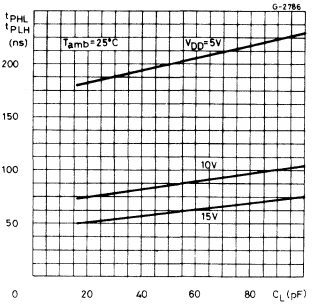
Minimum output high (source) current characteristics



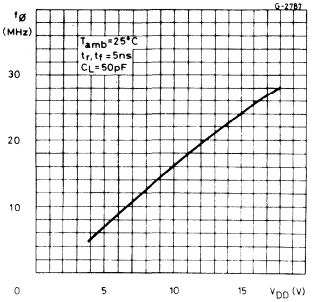
Typical propagation delay time vs. load capacitance (CLOCK or SET to Q CLOCK or RESET to $\overline{Q}$)



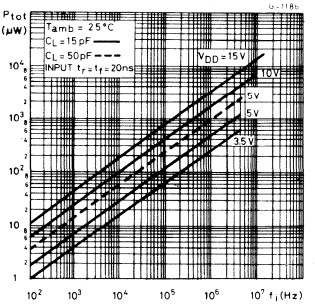
Typical propagation delay time vs. load capacitance (SET to $\overline{Q}$ or RESET to Q)



Typical maximum clock frequency vs. supply voltage



Typical power dissipation device vs. frequency



COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

8-STAGE STATIC SHIFT REGISTERS: 4014B-SYNCHRONOUS PARALLEL OR SERIAL INPUT/SERIAL OUTPUT 4021B-ASYNCHRONOUS PARALLEL INPUT OR SYNCHRONOUS SERIAL INPUT/ SERIAL OUTPUT

- MEDIUM-SPEED OPERATION -12 MHz (TYP.) CLOCK RATE AT V_{DD}-V_{SS}= 10V
- FULLY STATIC OPERATION
- 8 MASTER-SLAVE FLIP-FLOPS PLUS OUTPUT BUFFERING AND CONTROL GATING
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS

The **HCC 4014B, HCC 4021B** (extended temperature range) and the **HCF 4014B, HCF 4021B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4014B** and **HCC/HCF 4021B** series types are 8-stage parallel-or serial-input/serial-output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D type, master-slave flip-flop in addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the **HCC/HCF 4014B**. In the **HCC/HCF 4021B** serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the **HCC/HCF 4021B**, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple package is permitted.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

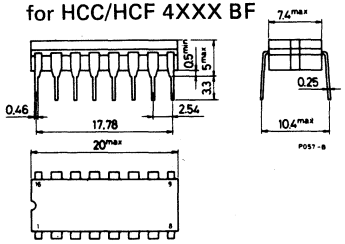
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

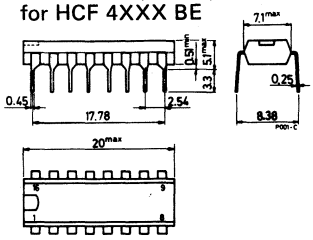
HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

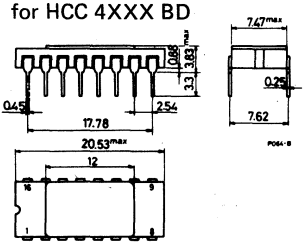
Dual in-line ceramic package for HCC/HCF 4XXX BF



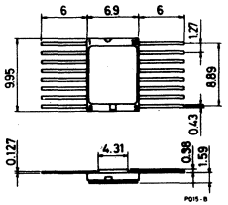
Dual in-line plastic package for HCF 4XXX BE



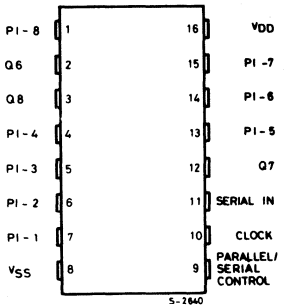
Dual in-line ceramic package for HCC 4XXX BD



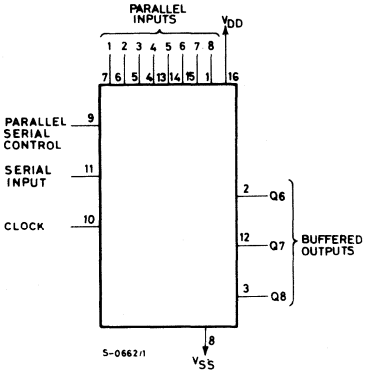
Ceramic flat package for HCC 4XXX BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

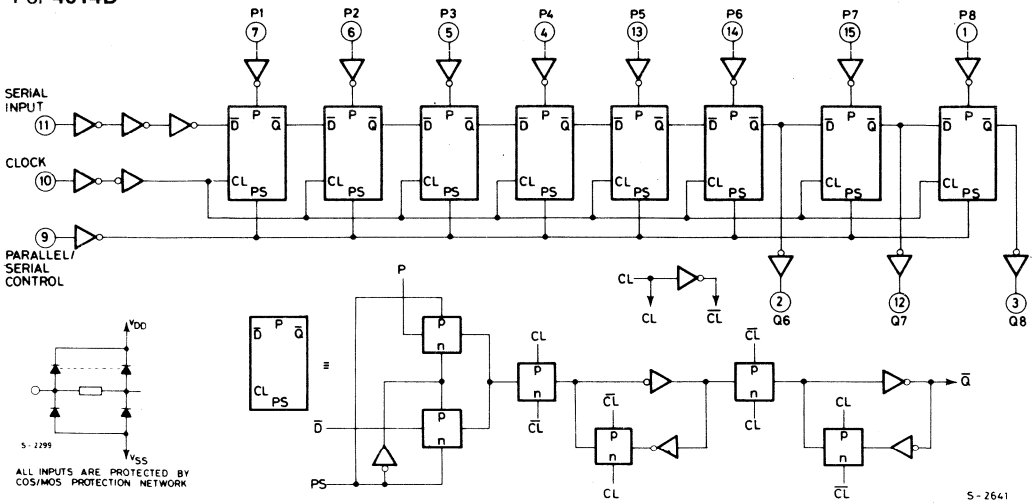


RECOMMENDED OPERATING CONDITIONS

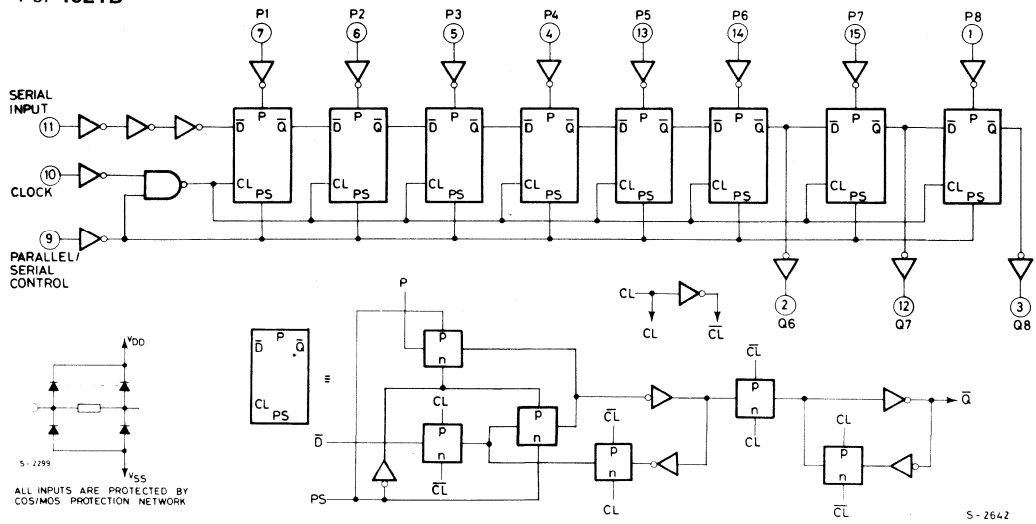
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAMS

For **4014B**



For **4021B**



TRUTH TABLES

For 4014B

CL	Serial Input	Parallel/ Serial Control	PI-1	PI-n	Q_1 (Internal)	Q_n	
⌐	X	1	0	0	0	0	
⌐	X	1	1	0	1	0	
⌐	X	1	0	1	0	1	
⌐	X	1	1	1	1	1	
⌐	0	0	X	X	0	Q_{n-1}	
⌐	1	0	X	X	1	Q_{n-1}	I
⌙	X	X	X	X	Q_1	Q_n	NC

X = DON'T CARE CASE
NC = NO CHANGE

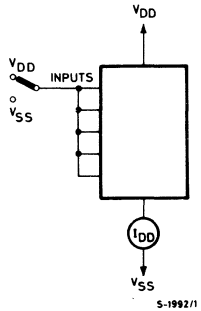
For 4021B

CL	Serial Input	Parallel/ Serial Control	PI-1	PI-n	Q_1 (Internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
⌐	0	0	X	X	0	Q_{n-1}	
⌐	1	0	X	X	1	Q_{n-1}	
⌙	X	0	X	X	Q_1	Q_n	N

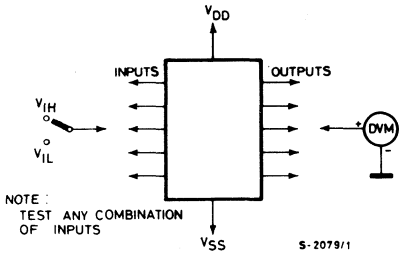
X = DON'T CARE CASE
NC = NO CHANGE

TEST CIRCUITS

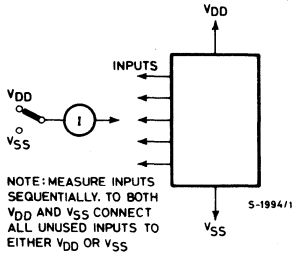
Quiescent device current



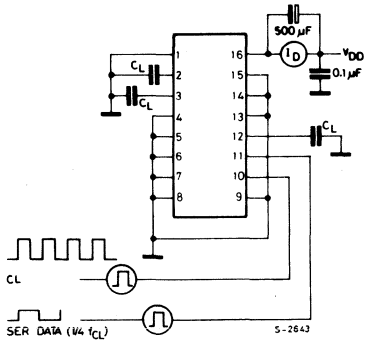
Noise immunity



Input leakage current



Dynamic power dissipation



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		± 0.1		$±10^{-5}$	±0.1		± 1	μA
C_I	Input capacitance			Any input						5	7.5			pF

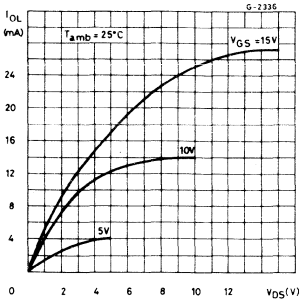
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

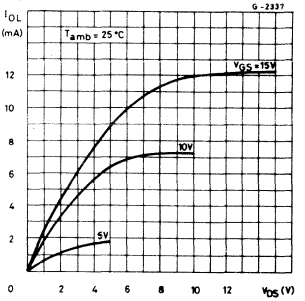
Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time	5		160	320	ns
		10		80	160	
		15		60	120	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}*	Maximum clock input frequency	5	3	6		MHz
		10	6	12		
		15	8.5	17		
t_W	Clock pulse width	5	180	90		ns
		10	80	40		
		15	50	25		
t_r, t_f	Clock input rise or fall time	5			15	μs
		10			15	
		15			15	
t_{setup}	Setup time, serial input (ref. to CL)	5	120	60		ns
		10	80	40		
		15	60	30		
t_{setup}	Setup time, parallel inputs (4014B) (ref. to CL)	5	80	40		ns
		10	50	25		
		15	40	20		
t_{setup}	Setup time, parallel inputs (4021B) (ref. to CL)	5	50	25		ns
		10	30	15		
		15	20	10		
t_{setup}	Setup time, parallel/serial control (4014B) (ref. to CL)	5	180	90		ns
		10	80	40		
		15	60	30		
t_{hold}	Hold time, serial in, parallel in, parallel/serial control	5	0			ns
		10	0			
		15	0			
t_{WH}	P/S Pulse width (4021B)	5	160	80		ns
		10	80	40		
		15	50	25		
t_{REM}	P/S Removal, time (4021B) (ref. to CL)	5	280	140		ns
		10	140	70		
		15	100	50		

* If more then one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

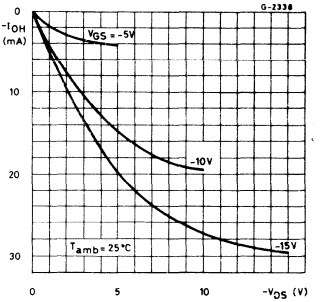
Typical output low (sink) current characteristics



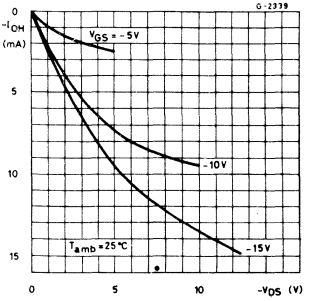
Minimum output low (sink) current characteristics



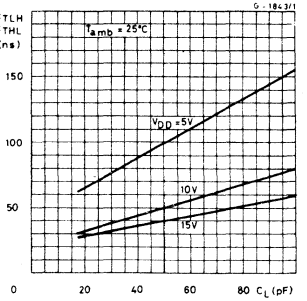
Typical output high (source) current characteristics



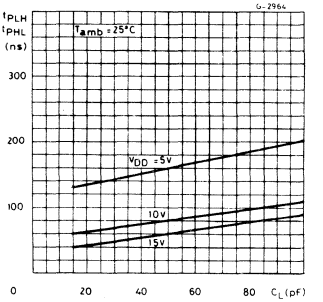
Minimum output high (source) current characteristics



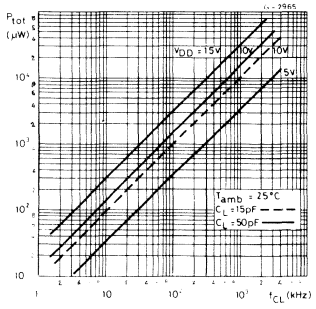
Typical transition time vs. load capacitance



Typical propagation delay time vs. load capacitance



Typical dynamic power dissipating vs. clock input frequency



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

DUAL 4-STAGE STATIC SHIFT REGISTER WITH SERIAL INPUT/PARALLEL OUTPUT

- QUIESCENT CURRENT SPECIFIED TO 20V
- MAX. INPUT LEAKAGE CURRENT 1 μA @ 18V (FULL TEMP. RANGE)
- HIGH NOISE IMMUNITY
- MEDIUM SPEED OPERATION: 12 MHz (TYP.) CLOCK RATE at V_{DD}-V_{SS}= 10V
- FULLY STATIC OPERATION
- 8 MASTER-SLAVE FLIP-FLOPS PLUS INPUT AND OUTPUT BUFFERING
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4015B** (extended temperature range) and **HCF 4015B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4015B** consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one **HCC/HCF 4015B** package, or to more than 8 stages using additional **HCC/HCF 4015B**'s is possible.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

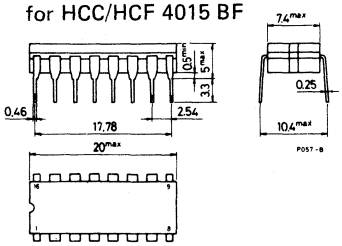
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

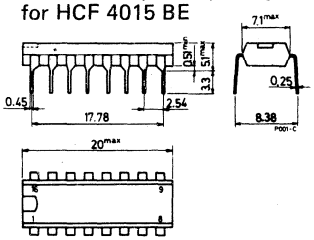
HCC 4015 BD for dual in-line ceramic package
HCC 4015 BF for dual in-line ceramic package, frit seal
HCC 4015 BK for ceramic flat package
HCF 4015 BE for dual in-line plastic package
HCF 4015 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

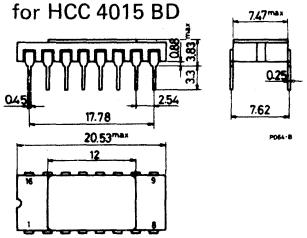
Dual in-line ceramic package for HCC/HCF 4015 BF



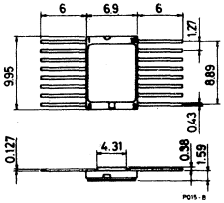
Dual in-line plastic package for HCF 4015 BE



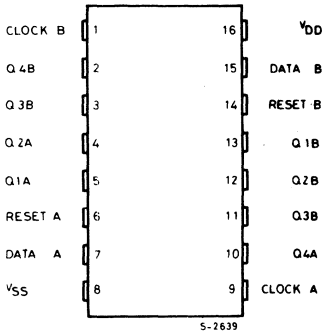
Dual in-line ceramic package for HCC 4015 BD



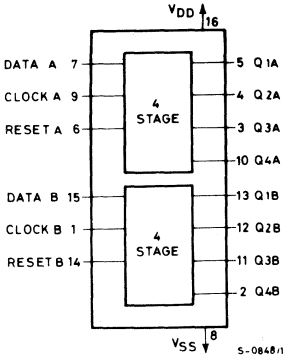
Ceramic flat package for HCC 4015 BK



CONNECTION DIAGRAM



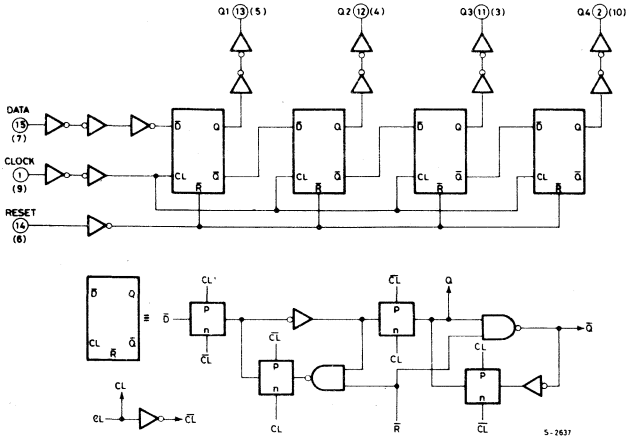
FUNCTIONAL DIAGRAM

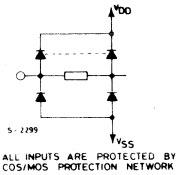


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM

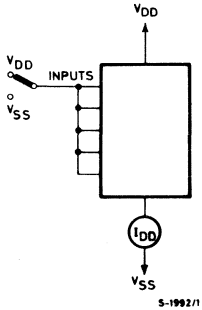




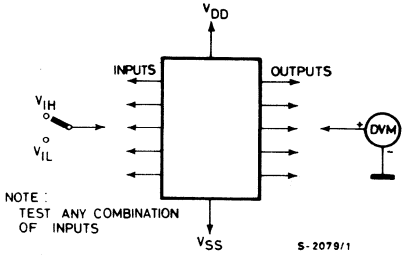
CL	D	R	Q_1	Q_n
⌒	0	0	0	Q_n-1
⌒	1	0	1	Q_n-1
⌒	X	0	Q_1	Q_n- (No.change)
X	X	1	0	0

TEST CIRCUITS

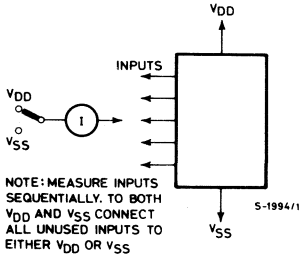
Quiescent device current



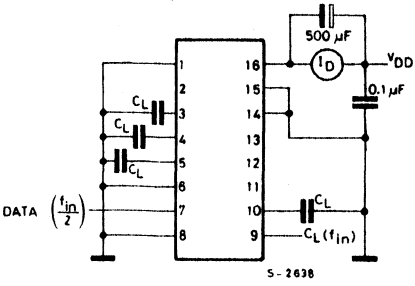
Input current



Input voltage



Power dissipation



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_i**	Input capacitance									5	7.5			pF

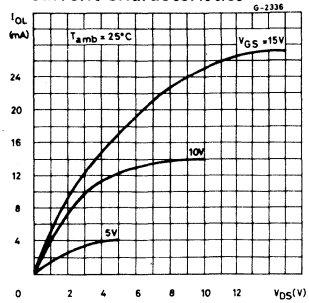
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

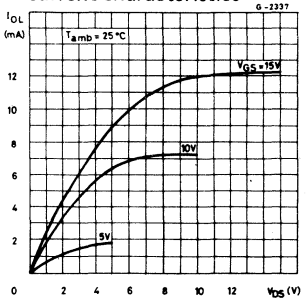
Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time (Carry Out or Decoded out Lines)	5		160	320	ns
		10		80	160	
		15		60	120	
t_{THL}, t_{TLH}	Transition time (Carry Out or Decoded Out Lines)	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}	Maximum clock input frequency	5	3	6		MHz
		10	6	12		
		15	8.5	17		
t_W	Clock pulse width	5	180	90		ns
		10	80	40		
		15	50	25		
t_r, t_f*	Clock input rise or fall time	5			15	μs
		10			15	
		15			15	
t_{setup}	Data setup time	5	70	35		ns
		10	40	20		
		15	30	15		
RESET OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time	5		200	400	ns
		10		100	200	
		15		80	160	
t_W	Reset pulse width	5	200	100		ns
		10	80	40		
		15	60	30		

* If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

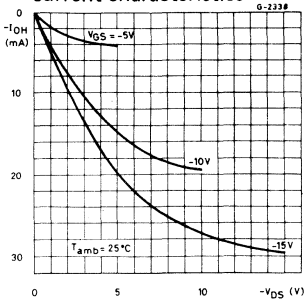
Typical output low (sink) current characteristics



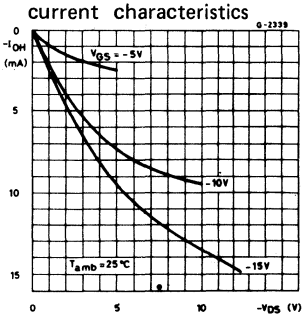
Minimum output low (sink) current characteristics



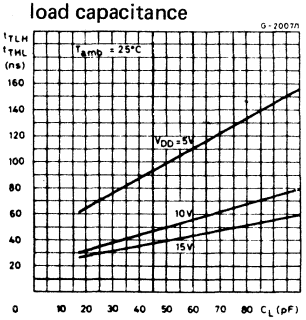
Typical output high (source) current characteristics



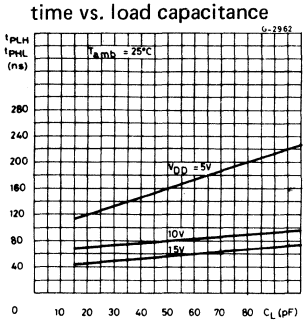
Minimum output high (source) current characteristics



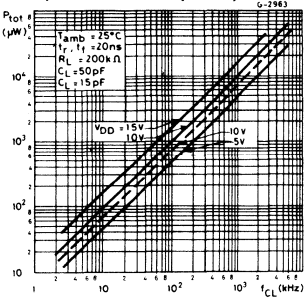
Typical transition time vs. load capacitance



Typical propagation delay time vs. load capacitance



Typical dynamic power dissipation vs. frequency



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

QUAD BILATERAL SWITCH

- 20V DIGITAL OR ± 10V PEAK-TO-PEAK SWITCHING
- 280Ω TYPICAL ON RESISTANCE FOR 15V OPERATION
- SWITCH ON RESISTANCE MATCHED TO WITHIN 10Ω TYP. OVER 15V SIGNAL INPUT RANGE
- HIGH ON/OFF OUTPUT-VOLTAGE RATIO: 65 dB TYP. @ f_{is}= 10 kHz, R_L= 10 kΩ
- HIGH DEGREE OF LINEARITY: < 0.5% DISTORTION TYP. @ f_{is}= 1 KHz, V_{is}= 5 V_{pp}, V_{DD}-V_{SS} ⩾ 10V, R_L= 10 kΩ
- EXTREMELY LOW OFF SWITCH LEAKAGE RESULTING IN VERY LOW OFFSET CURRENT AND HIGH EFFECTIVE OFF RESISTANCE: 100 pA TYP. @ V_{DD}-V_{SS}= 18V, T_{amb}= 25°C
- EXTREMELY HIGH CONTROL IMPUT IMPEDANCE (CONTROL CIRCUIT ISOLATED FROM SIGNAL CIRCUIT 10^{12} Ω TYP.)
- LOW CROSSTALK BETWEEN SWITCHES: -50 dB TYP. @ f_{is}= 0.9 MHz, R_L= 1 kΩ
- MATCHED CONTROL-INPUT TO SIGNAL-OUTPUT CAPACITANCE: REDUCES OUTPUT SIGNAL TRANSIENTS
- FREQUENCY RESPONSE, SWITCH ON = 40 MHz (TYP.)
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT 1 μA AT 18V (FULL PACKAGE TEMP. RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4016B** (extended temperature range) and **HCF 4016B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4016B** Series types are quad bilateral switches intended for the transmission or multiplexing of analog or digital signals. Each of the four independent bilateral switches has a single control signal input which simultaneously biases both the p and n device in a given switch ON or OFF.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

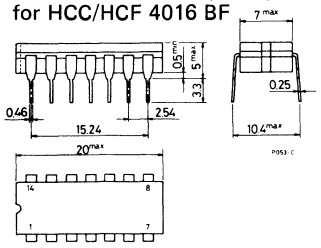
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

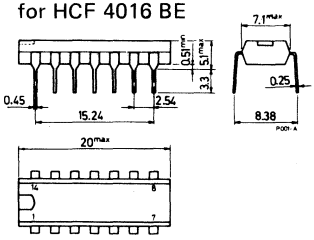
HCC 4016 BD for dual in-line ceramic package
HCC 4016 BF for dual in-line ceramic package, frit seal
HCC 4016 BK for ceramic flat package
HCF 4016 BE for dual in-line plastic package
HCF 4016 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

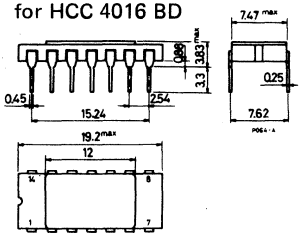
Dual in-line ceramic package for HCC/HCF 4016 BF



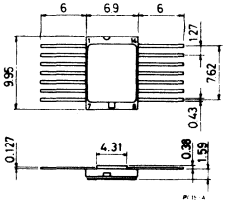
Dual in-line plastic package for HCF 4016 BE



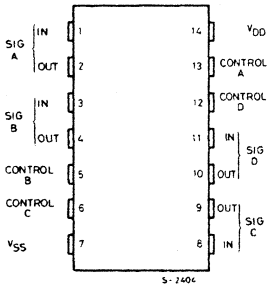
Dual in-line ceramic package for HCC 4016 BD



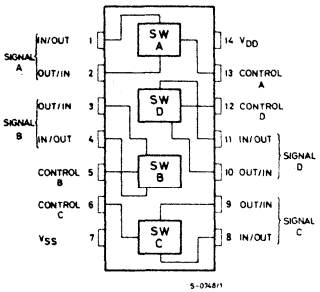
Ceramic flat package for HCC 4016 BK



CONNECTION DIAGRAM

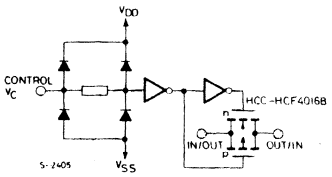


FUNCTIONAL DIAGRAM



SCHEMATIC DIAGRAM

1 of 4 identical section



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions				Values							Unit
			$V_C = V_{DD}$	V_{SS} (V)	V_{DD} (V)	T_{Low} (*)		25°C			T_{High} (*)		
						Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L Quiescent device current (all switches ON or all switches OFF)					5		0.25		0.01	0.25		7.5	μA
					10		0.5		0.01	0.5		15	
					15		1		0.01	1		30	
					20		5		0.02	5		150	
SWITCH					V_{IS}								
R_{ON} Resistance	HCC	R_L = 10 kΩ•	+ 7.5	- 7.5	+7.5		360		200	400		600	Ω
					-7.5		360		200	400		600	
					±0.25		775		280	850		1230	
	HCF				+7.5		370		200	400		520	
					-7.5		370		200	400		520	
					±0.25		790		280	850		1080	
	HCC	R_L = 10 kΩ•	+ 5	- 5	+ 5		600		250	660		960	
					- 5		600		250	660		960	
					±0.25		1870		580	2000		2600	
	HCF				+ 5		610		250	660		840	
					- 5		610		250	660		840	
					±0.25		1900		580	2000		2380	
	HCC	R_L = 10 kΩ•	+ 15	0	+15		360		200	400		600	
					+0.25		360		200	400		600	
					+9.3		775		300	850		1230	
	HCF		+ 15	0	+15		370		200	400		520	
					+0.25		370		200	400		520	
					+9.3		790		300	800		1080	
	HCC	R_L = 10 kΩ•	+ 10	0	+10		600		250	660		960	
					+0.25		600		250	660		960	
					+5.6		1870		560	2000		2600	
	HCF		+ 10	0	+10		610		250	660		840	
					+0.25		610		250	660		840	
					+5.6		1900		560	2000		2380	
ΔON Resistance between any 2 of 4 switches		R_L = 10 kΩ•	+7.5	-7.5	±7.5				10				Ω
			+ 5	- 5	± 5				15				
Input or output leakage current switch OFF (effective OFF resistance)			V_{DD}	$V_C = V_{SS}$									nA
			+ 18	0					10^{-3}	± 100			

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions	V_{DD} (V)	Values							Unit
			T_{Low} (*)		25°C			T_{High} (*)		
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
C_I Input capacitance	V_{CC}= V_{SS}= -5	+ 5				4				pF
C_O Output capacitance						4				
C_{IO} Feedthrough						0.2				
CONTROL (V_C)										
V_{TH} Switch threshold voltage	I_{IS}= 10 μA	5	1		1	2.25		1		V
		10	2		2	4.5		2		
		15	2		2	6.75		2		
I_I Input current	$V_{IS} \leqslant V_{DD}$	18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
C_i Input capacitance						5	7.5			pF

* T_{Low}= - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High}= +125°C for **HCC** device; + 85°C for **HCF** device.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF all input square wave rise and fall times = 20 ns)

Parameter	Test conditions							Values		Unit
	V_C (V)	R_L (kΩ)	f_i (KHz)	V_I (V)	V_{SS} (V)	V_{DD} (V)		Typ.	Max.	
SWITCH										
t_{pd} Propagation delay time (Signal input to output)	= V_{DD}	10		10sq. Wave	GND	5		40	100	ns
						10		20	50	
						15		15	40	
Crosstalk between any 2 of 4 switches (f @ -50 dB) 20 log 10 $\frac{V_{O(B)}}{V_{I(A)}}$ = -50 dB	$V_{C(A)}$=V_{DD}= +5 $V_{C(B)}$=V_{SS}= -5	1		$V_{I(A)}$ =5p-p				0.9		MHz
Frequency response switch "ON"(Sine wave input) at 20 log 10 $\frac{V_O}{V_I}$ = -3 dB	= V_{DD} = + 5	1		5p-p	- 5			40		MHz
Feedthrough (Switch OFF) at 20 log 10 $\frac{V_O}{V_I}$ = -50 dB	= V_{SS} = - 5	1		-5p-p		5		1.25		MHz
Sine wave distortion	= V_{DD} = 5	10	1	5p-p	- 5			0.4		%

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions							Values		Unit
	V_C (V)	R_L (kΩ)	f_i (KHz)	V_I (V)	V_{SS} (V)	V_{DD} (V)		Typ.	Max.	
CONTROL (V_C)										
Propagation delay: (Turn ON Control to Output)	V_{DD}-V_{SS} (Sq. Wave)	1		V_{DD} or V_{SS}		5	V_{DD}-V_{SS}=10V	35	70	ns
						10		20	40	
						15		15	30	
Max. Allowable control input repetition rate	10 (Sq. Wave)	1		V_{DD}	GND	10		10		MHz
Crosstalk (Control input to signal output)	10 (sq, Wave)	10			GND	10		50		mV

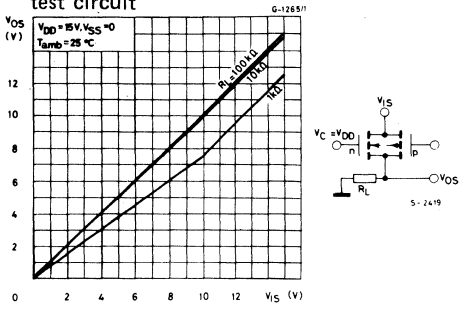
(▲) Symmetrical about 0V (●) For all test conditions.

TYPICAL "ON" RESISTANCE CHARACTERISTICS, $T_A = 25°C$

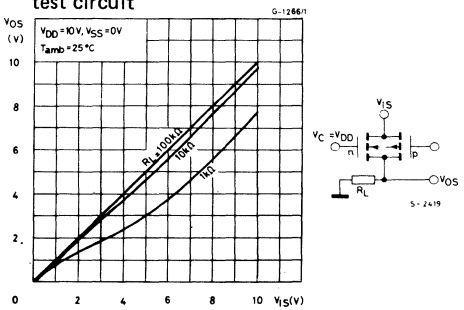
CHARAC-TERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1 kΩ		R_L = 10 kΩ		R_L = 100 kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+ 15	0	200	+ 15	200	+ 15	180	+ 15
			200	0	200	0	200	0
R_{ON} (max.)	+ 15	0	300	+ 11	300	+ 9.3	320	+ 9.2
R_{ON}	+ 10	0	290	+ 10	250	+ 10	240	+ 10
			290	0	250	0	300	0
R_{ON} (max.)	+ 10	0	500	+ 7.4	560	+ 5.6	610	+ 5.5
R_{ON}	+ 5	0	860	+ 5	470	+ 5	450	+ 5
			600	0	580	0	800	0
R_{ON} (max.)	+ 5	0	1.7k	+ 4.2	7k	+ 2.9	33k	+ 2.7
R_{ON}	+ 7.5	- 7.5	200	+ 7.5	200	+ 7.5	180	+ 7.5
			200	- 7.5	200	- 7.5	180	- 7.5
R_{ON} (max.)	+ 7.5	- 7.5	290	± 0.25	280	± 25	400	± 0.25
R_{ON}	+ 5	- 5	260	+ 5	250	+ 5	240	+ 5
			310	- 5	250	- 5	240	- 5
R_{ON} (max.)	+ 5	- 5	600	± 0.25	580	± 0.25	760	± 0.25
R_{ON}	† 2.5	-2.5	590	+ 2.5	450	+ 2.5	490	+ 2.5
			720	- 2.5	520	- 2.5	520	- 2.5
R_{ON} (max.)	+ 2.5	- 2.5	232k	± 0.25	300k	± 0.25	870k	± 0.25

* Variation from a perfect switch, R_{ON}= 0Ω.

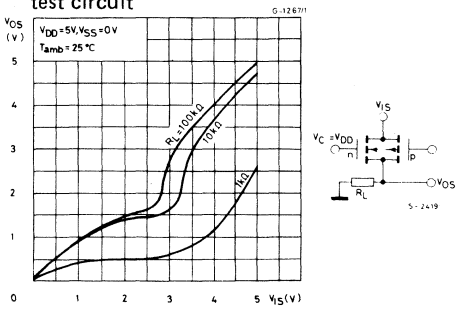
Typical "ON" characteristics for 1 of 4 switches with V_{DD}= +15V, V_{SS}= 0V, and test circuit



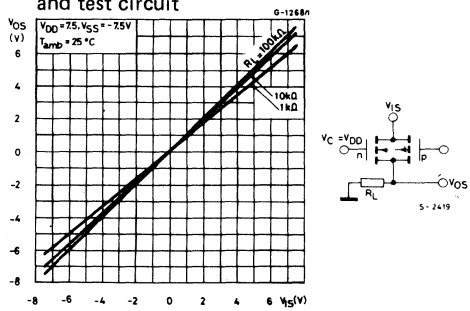
Typical "ON" characteristics for 1 of 4 switches with V_{DD}= +10V. V_{SS}= 0V, and test circuit



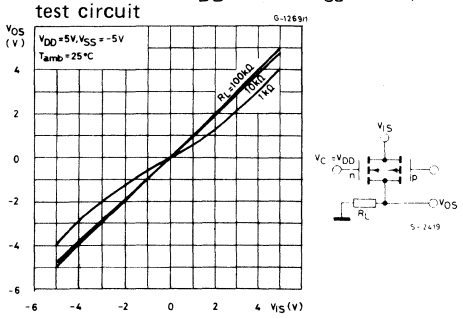
Typical "ON" characteristics for 1 of 4 switches with V_{DD}= +5V, V_{SS}= 0V, and test circuit



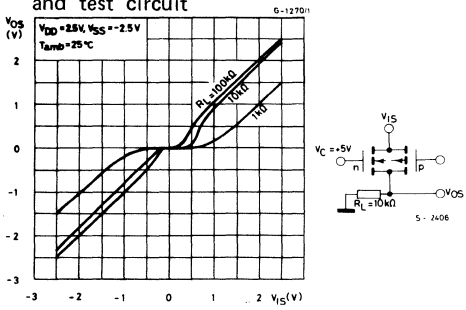
Typical "ON" characteristics for 1 of 4 switches with V_{DD}= +7.5V, V_{SS}= -7.5V, and test circuit



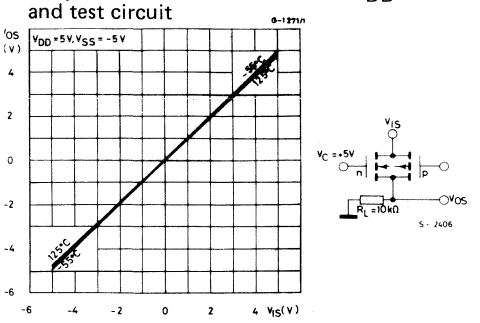
Typical "ON" characteristics for 1 of 4 switches with V_{DD}= +5V, V_{SS}= -5V, and test circuit



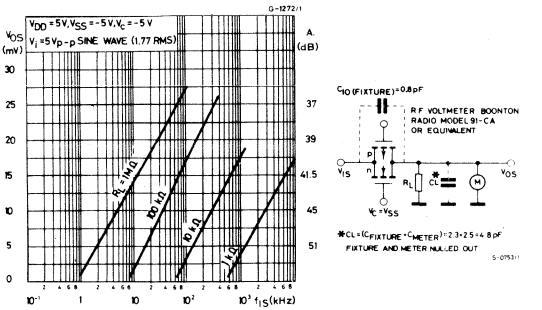
Typical "ON" characteristics for 1 of 4 switches with V_{DD}= +2.5V, V_{SS}= -2.5V and test circuit



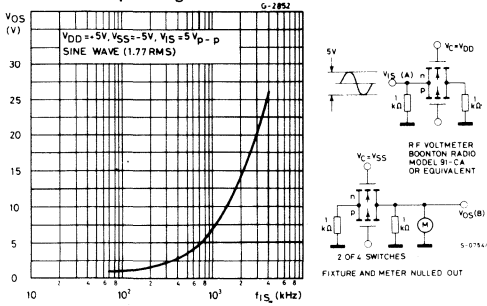
Typical "ON" characteristics as function of temp. for 1 of 4 switches with V_{DD} = +5V and test circuit



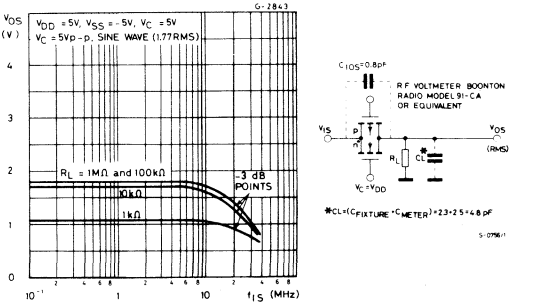
Typical feedthru vs. frequency-switch "OFF" and test circuit



Typical crosstalk between switch circuits in the same package

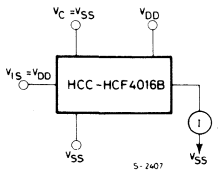


Typical switch frequency response-sw: "ON" and test circuit



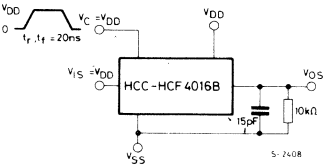
TEST CIRCUITS

"OFF" switch input or put leakage current



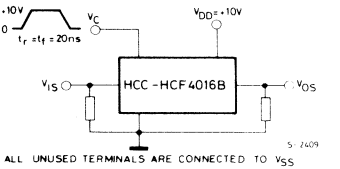
ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}

Square-wave response



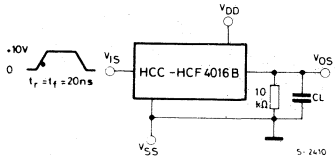
ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}

Crosstalk-control input to signal output



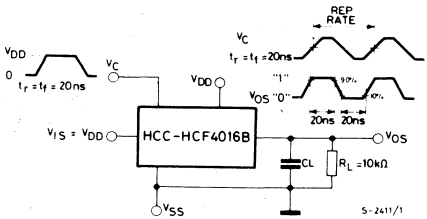
ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}

Propagation delay time signal input (V_{IS}) to signal output (V_{OS})



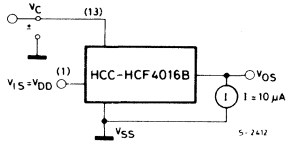
ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}

Max. allowable control-input repetition rate



ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}

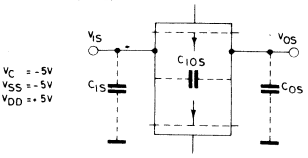
Switch threshold voltage



SWITCH THRESHOLD VOLTAGE IS DEFINED AS THE VOLTAGE APPLIED TO A TRANSMISSION GATE CONTROL WHICH CAUSES 10 μA OF TRANSMISSION GATE CURRENT.

Capacitance C_{IOS} and C_{OS}

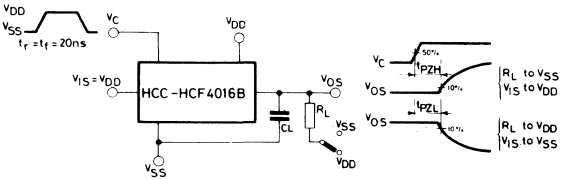
MEASURED ON BOONTON CAPACITANCE BRIDGE MODEL 75A (1MHz)



ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}

5-2413

Turn-On propagation delay-control input to output



ALL UNUSED TERMINALS ARE CONNECTED TO V_{SS}

5-2414/1

COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

COUNTER/DIVIDERS: 4017B - DECADE COUNTER WITH 10 DECODED OUTPUTS
4022B - OCTAL COUNTER WITH 8 DECODED OUTPUTS

- FULLY STATIC OPERATION
- MEDIUM SPEED OPERATION-12 MHz (TYP.) AT V_{DD}= 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4017B/4022B** (extended temperature range) and **HCF 4017B/4022B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4017B** and **HCC/HCF 4022B** are 5-stage and 4-stage Johnson counters having 10 and 8 decoded outputs, respectively. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times. These counters are advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson decade-counter configuration permits high-speed operation, 2-input decimal-decode gating, and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the **HCC/HCF 4017B** or every 8 clock input cycles in the **HCC/HCF 4022B** and is used to ripple-clock the succeeding device in a multi-device counting chain.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

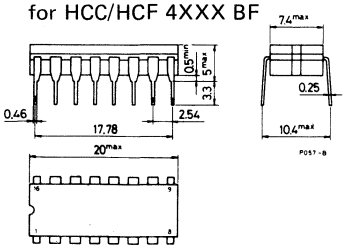
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

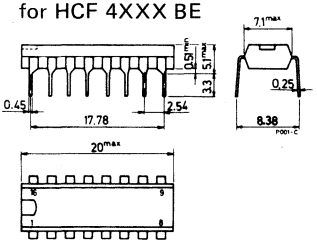
HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

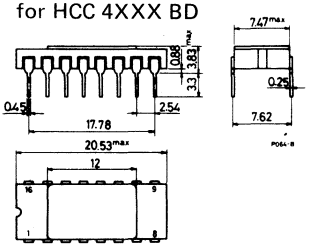
Dual in-line ceramic package
for HCC/HCF 4XXX BF



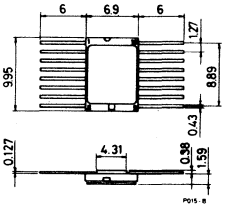
Dual in-line plastic package
for HCF 4XXX BE



Dual in-line ceramic package
for HCC 4XXX BD

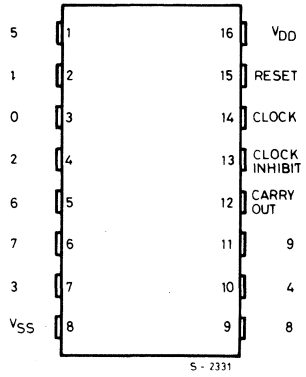


Ceramic flat package
for HCC 4XXX BK



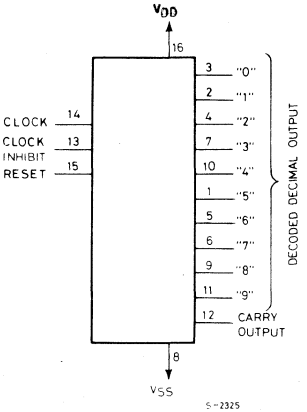
CONNECTION DIAGRAM

for **4017B**



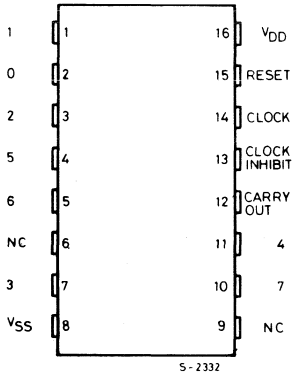
FUNCTIONAL DIAGRAM

for **4017B**



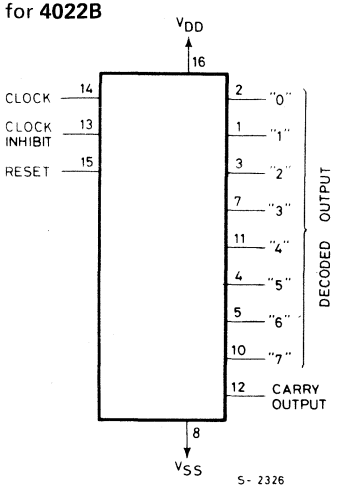
CONNECTION DIAGRAM

for **4022B**



FUNCTIONAL DIAGRAM

for **4022B**

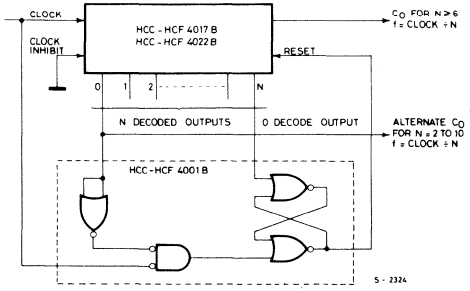


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

TYPICAL APPLICATIONS

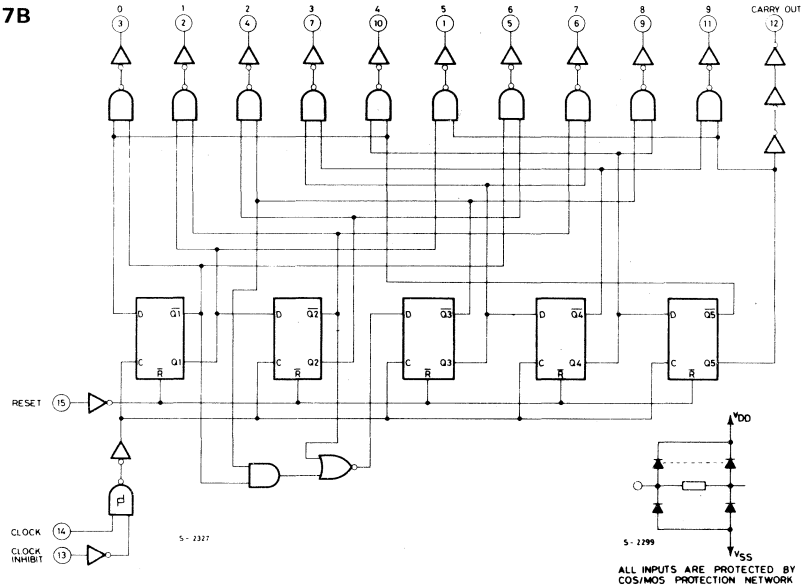
Divide by N counter ($N \leqslant 10$) with N decoded outputs



When the N^{th} decoded output is reached (N^{th} clock pulse) the S-R flip-flop (constructed from two NOR gates of the **HCC/HCF 4001B**) generates a reset pulse which clears the **HCC/HCF 4017B** to its zero count. At this time, if the N^{th} decoded output is greater than or equal to 6, the C_{OUT} line goes high to clock the next **HCC/HCF 4017B** counter section. The "0" decoded output also goes high at this time. Coincidence of the clock low and decoded "0" output high resets the S-R flip flop to enable the **HCC/HCF 4017B**. If the N^{th} decoded output is less than 6, the C_{OUT} line will not go high and, therefore, cannot be used. In this case "0" decoded output may be used to perform the clocking function for the next counter.

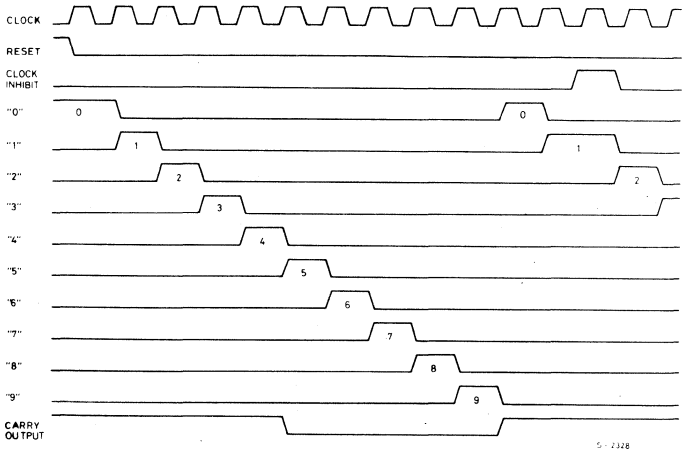
LOGIC DIAGRAM

for **4017B**



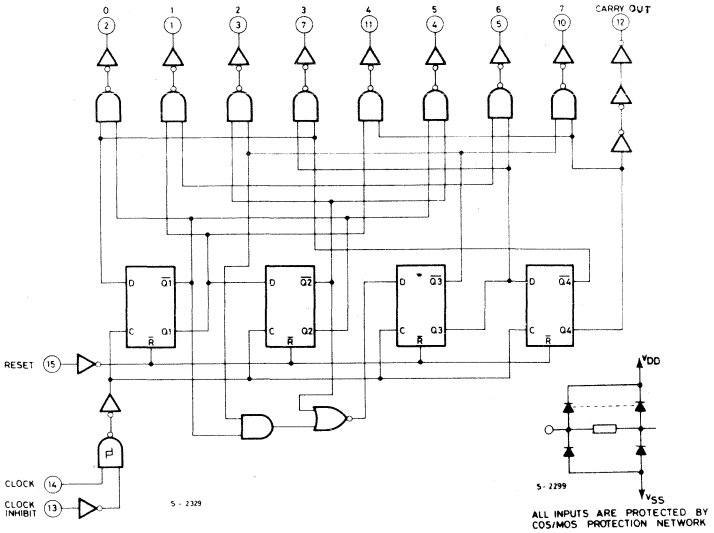
TIMING DIAGRAM

for **4017B**



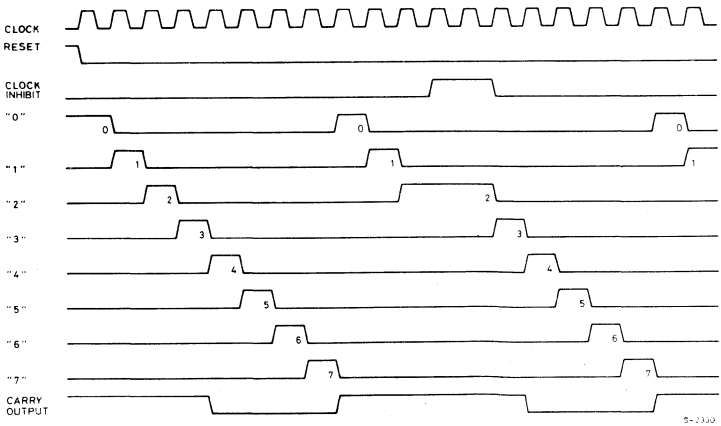
LOGIC DIAGRAM

for **4022B**



TIMING DIAGRAM

for **4022B**



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

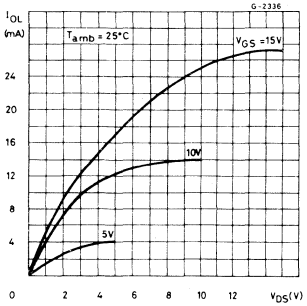
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD}= 0.3%/°C values, all input rise and fall time = 20 ns)

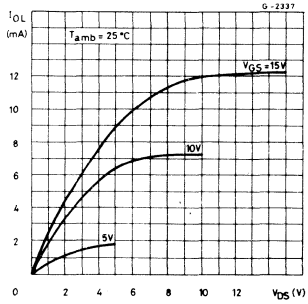
Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time (Carry Out or Decoded out Lines)	5		250		ns
		10		100		
		15		80		
t_{THL}, t_{TLH}	Transition time (Carry Out or Decoded Out Lines)	5		100		ns
		10		50		
		15		40		
f_{CL}*	Maximum clock input frequency	5		5		MHz
		10		12		
		15		16		
t_W	Minimum clock pulse width	5		100		ns
		10		45		
		15		30		
t_r, t_f	Clock input rise or fall time	5		Unlimited		μs
		10				
		15				
t_{setup}	Data setup time Minimum clock inhibit	5		175		ns
		10		75		
		15		50		
RESET OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time (Carry Out or Decode Out Lines)	5		250		ns
		10		100		
		15		80		
t_W	Minimum reset pulse width	5		200		ns
		10		100		
		15		75		
t_R	Minimum reset removal time	5		100		ns
		10		50		
		15		40		

* Measured with respect to carry output line.

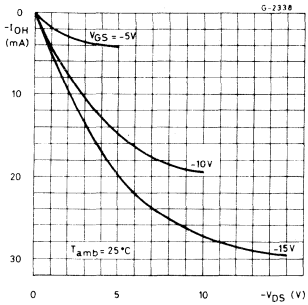
Typical output low (sink) current characteristics



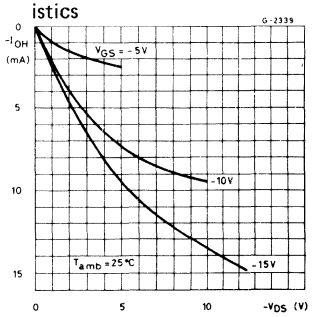
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics



Minimum output high (source) current characteristics



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

PRESETTABLE DIVIDE-BY-N COUNTER

- MEDIUM SPEED OPERATION -10 MHz (TYP.) AT V_{DD}-V_{SS}= 10V
- FULLY STATIC OPERATION
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4018B** (extended temperature range) and **HCF 4018B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4018B** types consist of 5 Johnson-Counter stages, buffered $\overline{Q}$ outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, $\overline{Q}1$ signals, respectively, back to the DATA input.
Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a **HCC/HCF 4011B** gate package to properly gate the feedback connection to the DATA input. Divide-by-functions greater than 10 can be achieved by use of multiple **HCC/HCF 4018B** units. The counter is advanced one count at the positive clock-signal transition. Schmitt Trigger action on the clock line permits unlimited clock rise and fall times. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperatura range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

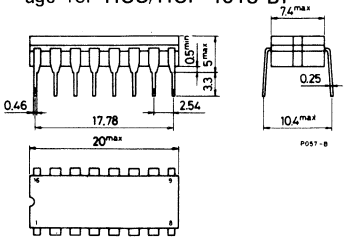
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

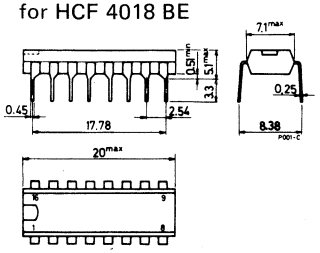
HCC 4018 BD for dual in-line ceramic package
HCC 4018 BF for dual in-line ceramic package, frit seal
HCC 4018 BK for ceramic flat package
HCF 4018 BE for dual in-line plastic package
HCF 4018 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

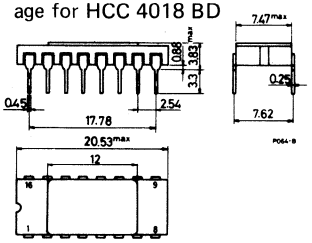
Dual in-line ceramic package for HCC/HCF 4018 BF



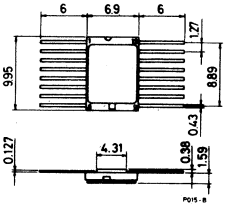
Dual in-line plastic package for HCF 4018 BE



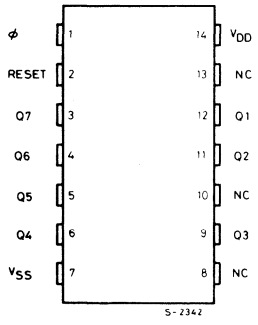
Dual in-line ceramic package for HCC 4018 BD



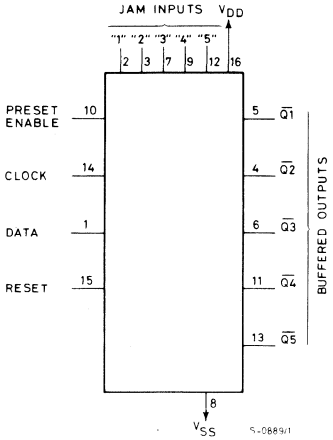
Ceramic flat package for HCC 4018 BK



CONNECTION DIAGRAM



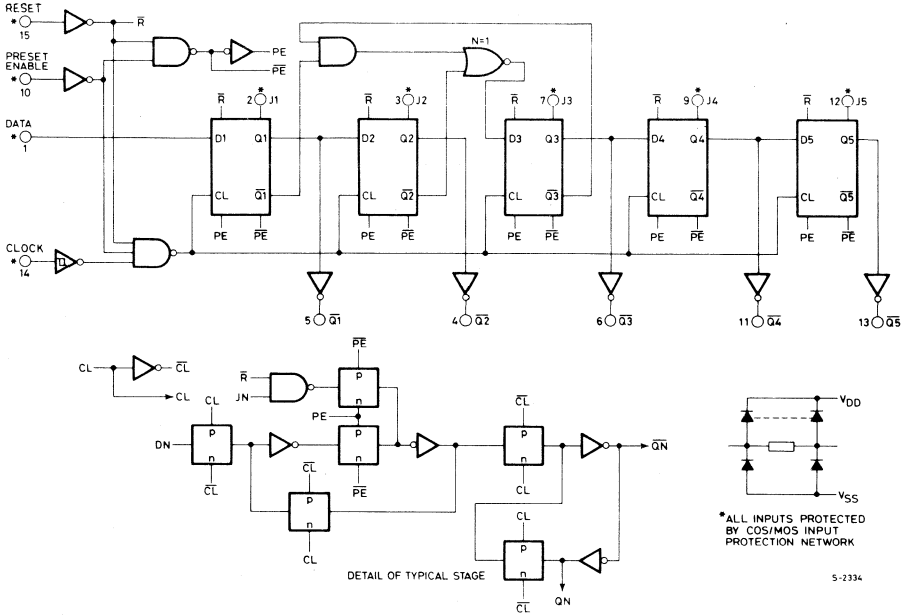
FUNCTIONAL DIAGRAM



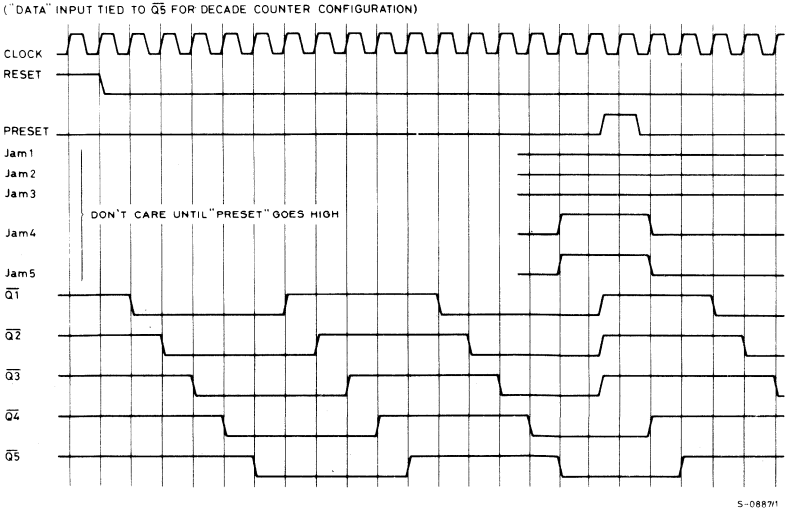
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM



TIMING DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (under recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		±1	μA
C_I**	Input capacitance									5	7.5			pF

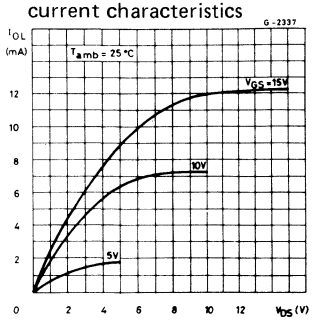
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

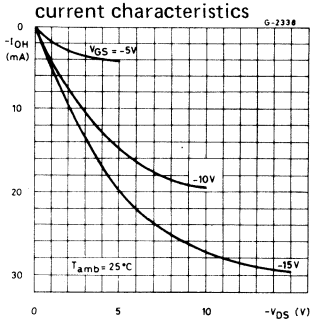
Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time	5		200	400	ns
		10		90	180	
		15		65	130	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}	Maximum clock input frequency	5	3	6		MHz
		10	7	14		
		15	8.5	17		
t_W	Clock input width	5	160	80		ns
		10	70	35		
		15	50	25		
t_r, t_f	Clock input rise or fall time	5	Unlimited			μs
		10				
		15				
t_{setup}	Data input Set-Up time	5	40	20		ns
		10	12	6		
		15	6	3		
t_H	Data input Hold-time	5	140	70		ns
		10	80	40		
		15	60	30		
PRESET* OR RESET OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time (Reset or Reset to $\overline{Q}$)	5		275	550	ns
		10		125	250	
		15		90	180	
t_W	Preset or reset pulse width	5	160	80		ns
		10	70	35		
		15	50	25		
t_R	Preset or reset removal time	5	80	40		ns
		10	30	15		
		15	20	10		

* At PRESET ENABLE OR JAM Inputs

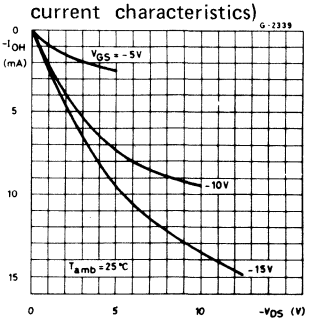
Minimum output low (sink) current characteristics



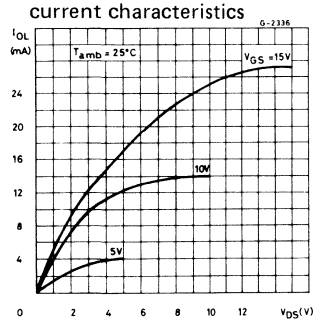
Typical output high (source) current characteristics



Minimum output high (source current characteristics)



Typical output low (sink) current characteristics

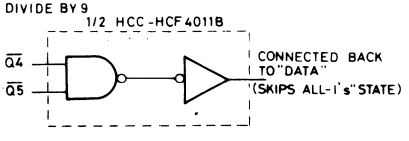


APPLICATION

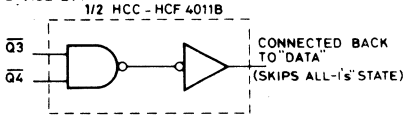
External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, 2 operation

DIVIDE BY 10	$\overline{Q}_5$	CONNECTED BACK TO "DATA"	NO EXTERNAL COMPONENTS REQUIRED
DIVIDE BY 8	$\overline{Q}_4$		
DIVIDE BY 6	$\overline{Q}_3$		
DIVIDE BY 4	$\overline{Q}_2$		
DIVIDE BY 2	$\overline{Q}_1$	NO CONNECTED	

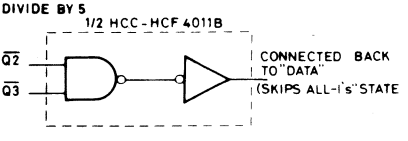
DIVIDE BY 9



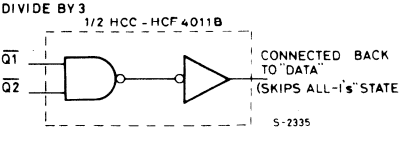
DIVIDE BY 7



DIVIDE BY 5



DIVIDE BY 3



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

QUAD AND/OR SELECT GATE

- MEDIUM SPEED OPERATION: $t_{PHL} = t_{PLH} = 60$ ns (TYP.) AT $C_L = 50$ pF, $V_{DD} = 10$V
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4019B** (extended temperature range) and **HCF 4019B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package.
The **HCC/HCF 4019B** types are comprised of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_a and K_b. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

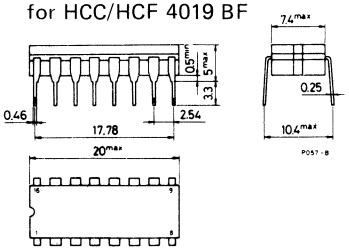
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

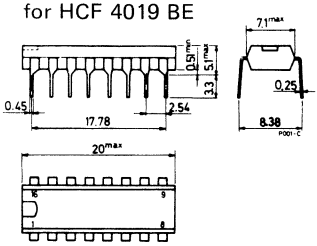
HCC 4019 BD for dual in-line ceramic package
HCC 4019 BF for dual in-line ceramic package, frit seal
HCC 4019 BK for ceramic flat package
HCF 4019 BE for dual in-line plastic package
HCF 4019 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

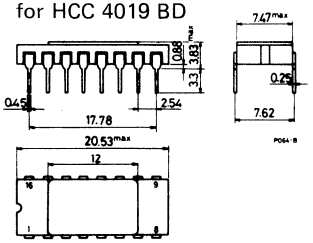
Dual in-line ceramic package for HCC/HCF 4019 BF



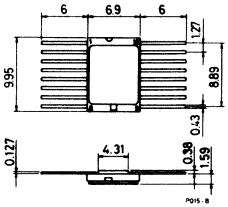
Dual in-line plastic package for HCF 4019 BE



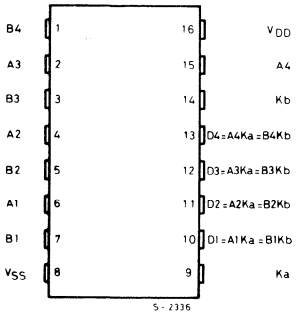
Dual in-line ceramic package for HCC 4019 BD



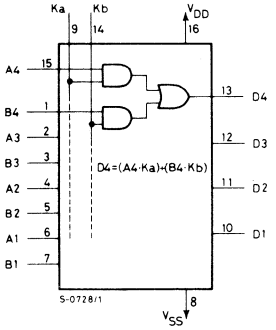
Ceramic flat package for HCC 4019 BK



CONNECTION DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

Ka	Kb	An	Bn	DN
1	X	1	X	1
1	X	0	X	0
X	1	X	1	1
X	1	X	0	0
0	0	X	X	0

X = Don't care

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

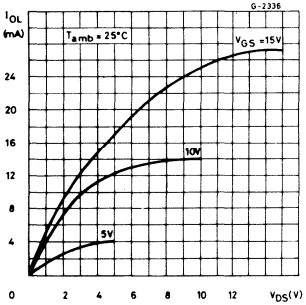
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I Input capacitance	All A and B inputs									5	7.5			pF
	Ka and Kb inputs									10	15			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

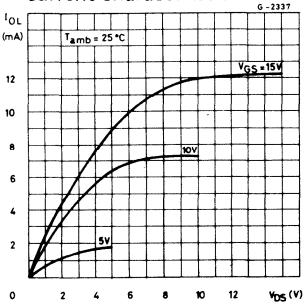
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
	V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time	5		150	300	ns
	10		60	120	
	15		50	100	
t_{TLH}, t_{THL} Transition time	5		100	200	ns
	10		50	100	
	15		40	80	

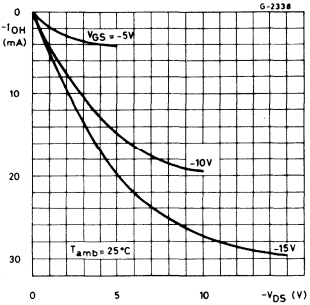
Typical output low (sink) current characteristics



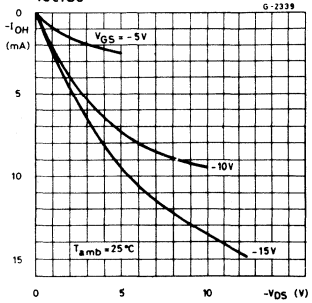
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics

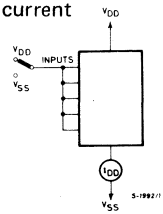


Minimum output high (source) current characteristics

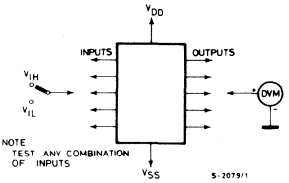


TEST CIRCUITS

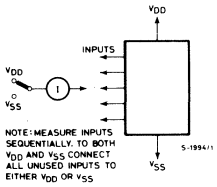
Quiescent device current



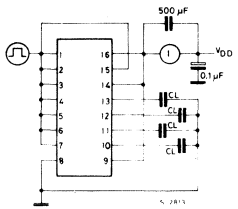
Input voltage



Input leakage current

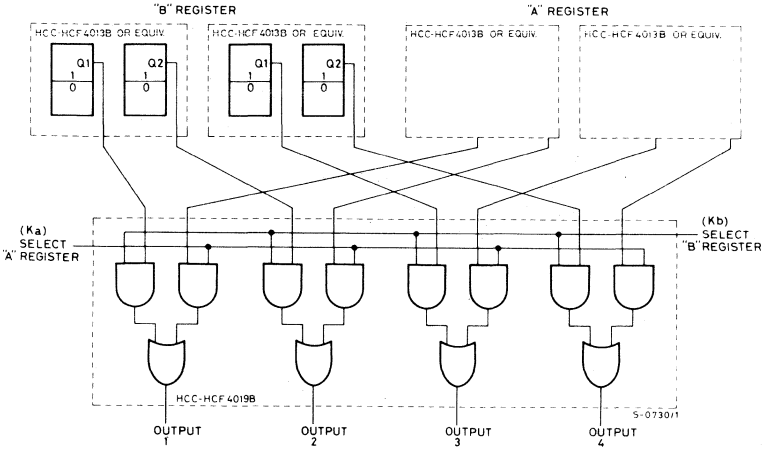


Dynamic power dissipation

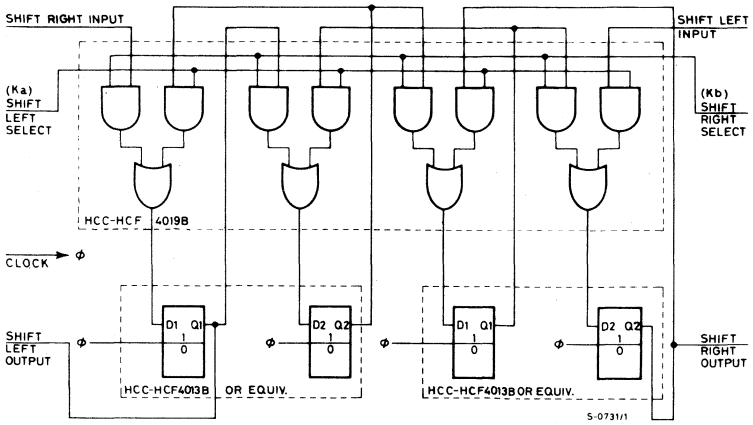


TYPICAL APPLICATIONS

AND-OR selected gating

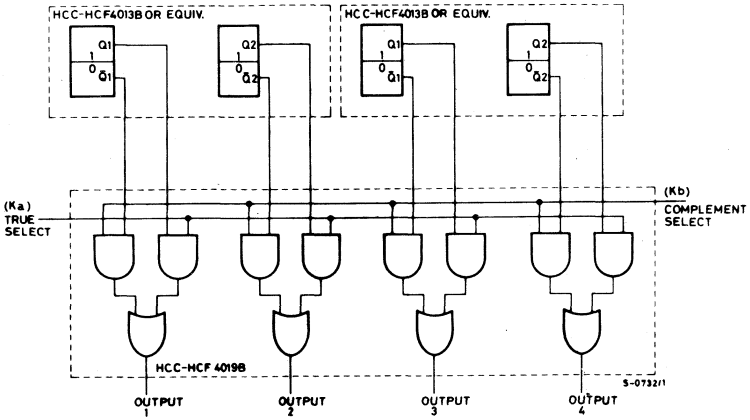


Shift left shift right register

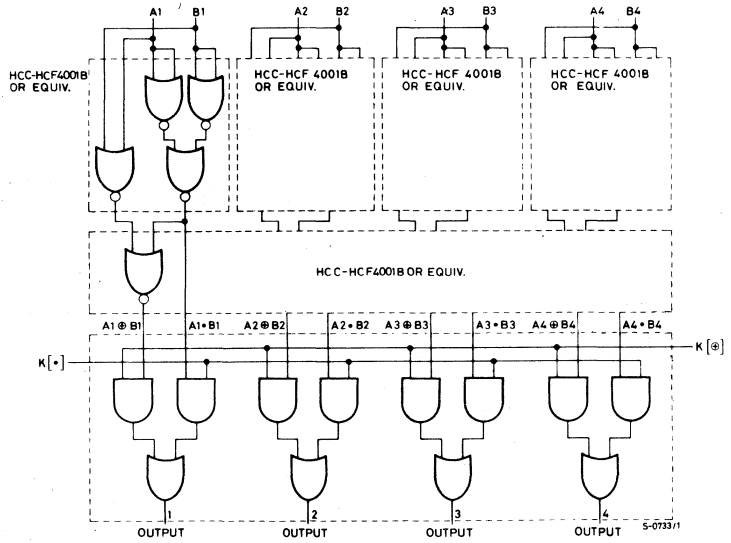


TYPICAL APPLICATIONS (continued)

True complement selector



AND-OR exclusive - OR selector



TRUTH TABLE

K [•]	K [⊕]	OUT
0	0	0
1	0	A - B
0	1	A ⊕ B
1	1	A + B

COS/MOS INTEGRATED CIRCUITS

HCC/HCF 4020B
HCC/HCF 4024B
HCC/HCF 4040B

PRELIMINARY DATA

RIPPLE-CARRY BINARY COUNTER/DIVIDERS: 4020B - 14 STAGE
4024B - 7 STAGE
4040B - 12 STAGE

- MEDIUM-SPEED OPERATION
- FULLY STATIC OPERATION
- COMMON RESET
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4XXXB** (extended temperature range) and **HCF 4XXXB** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line for **4024B** and 16-lead dual in-line for **4020B, 4040B.** The series types are supplied in plastic or ceramic dual in-line package and ceramic flat package.

The **HCC/HCF 4020B, 4024B**, and **4040B** are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros stage. Schmitt trigger action on the input-pulse line permits unlimited clock rise and fall times. All inputs and outputs are buffered.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

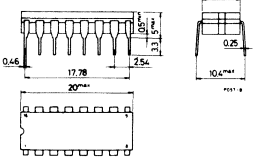
HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

HCC/HCF 4020B
HCC/HCF 4024B
HCC/HCF 4040B

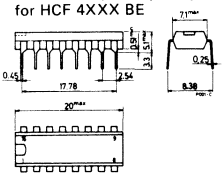
MECHANICAL DATA (dimensions in mm)

For **4020B** and **4040B**

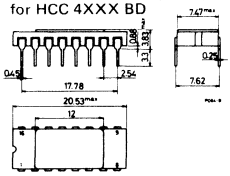
Dual in-line ceramic package for HCC/HCF 4XXX BF



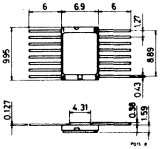
Dual in-line plastic package for HCF 4XXX BE



Dual in-line ceramic package for HCC 4XXX BD

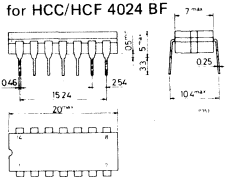


Ceramic flat package for HCC 4XXX BK

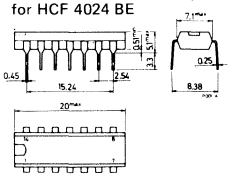


For **4024B**

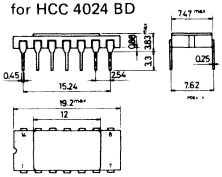
Dual in-line ceramic package for HCC/HCF 4024 BF



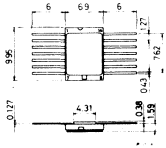
Dual in-line plastic package for HCF 4024 BE



Dual in-line ceramic package for HCC 4024 BD

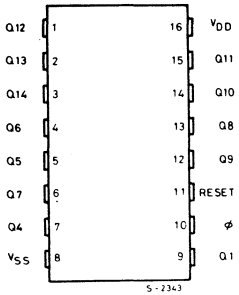


Ceramic flat package for HCC 4024 BK

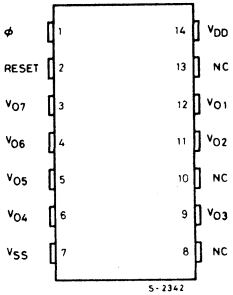


CONNECTION DIAGRAMS

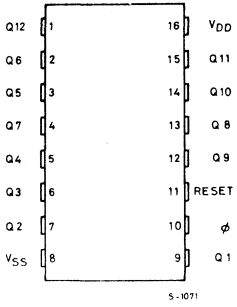
For **4020B**



For **4024B**



For **4040B**

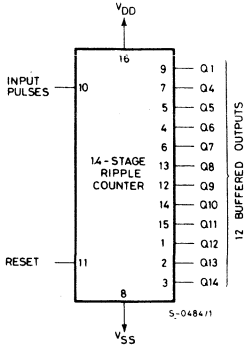


RECOMMENDED OPERATING CONDITIONS

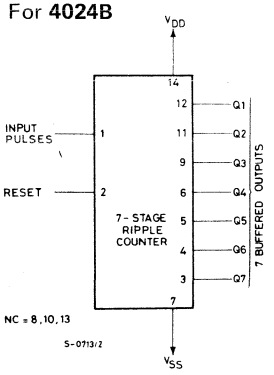
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

FUNCTIONAL DIAGRAMS

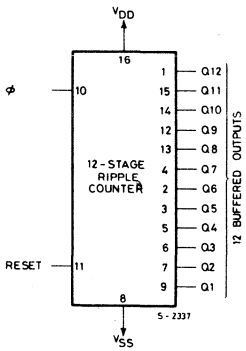
For **4020B**



For **4024B**

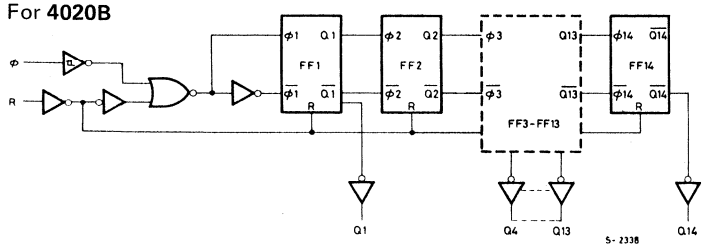


For **4040B**

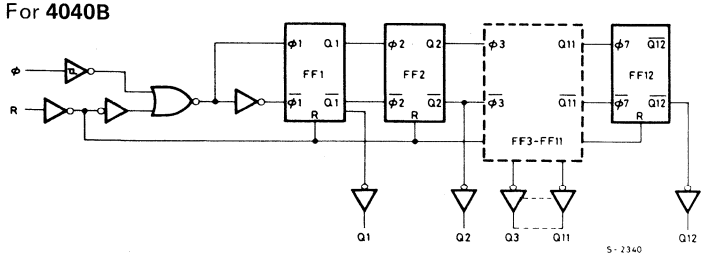


LOGIC DIAGRAMS

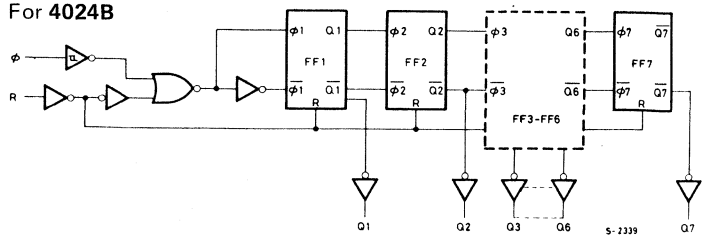
For **4020B**

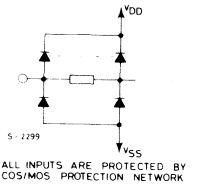


For **4040B**



For **4024B**





STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

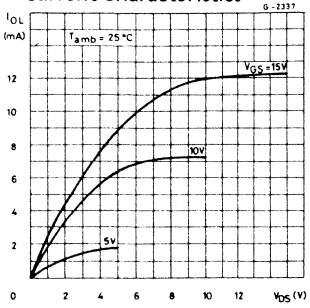
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}	Input leakage current		0/18	Any input		18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

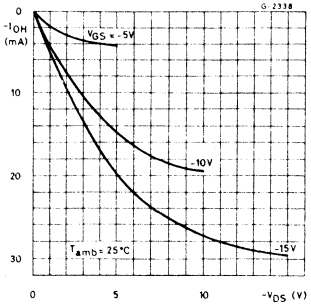
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
INPUT-PULSE OPERATION							
t_{PLH}, t_{PHL}	Propagation delay time (ϕ 1 to Q1 Out)		5		400		ns
			10		170		
			15		120		
t_{PLH}, t_{PHL}	Propagation delay time (Qn to Qn + 1)		5		200		ns
			10		85		
			15		60		
t_{TLH}, t_{THL}	Transition time		5		100		ns
			10		50		
			15		40		
t_W	Minimum input pulse width		5		70		ns
			10		30		
			15		20		
t_r, t_f	Input pulse rise and fall time		5	Unlimited			μs
			10				
			15				
f_{max}	Maximum clock input frequency		5		7		MHz
			10		16		
			15		24		
RESET OPERATION							
t_{PHL}	Propagation delay time		5		300		ns
			10		140		
			15		100		
t_W	Minimum reset pulse width		5		375		ns
			10		200		
			15		150		

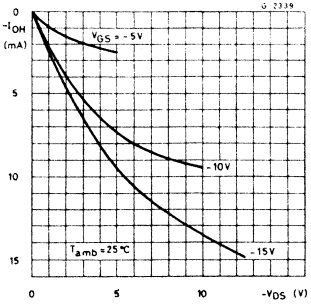
Minimum output low (sink) current characteristics



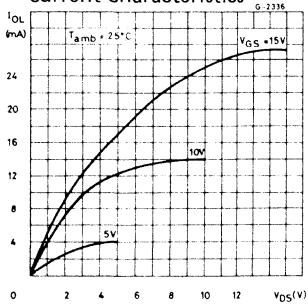
Typical output high (source) current characteristics



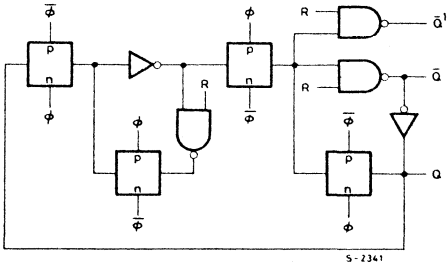
Minimum output high (source) current characteristics



Typical output low (sink) current characteristics



Detail of typical flip-flop stage



COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

DECADE COUNTERS/DIVIDERS WITH DECODED 7-SEGMENT DISPLAY OUTPUTS AND: DISPLAY ENABLE 4026B RIPPLE BLANKING 4033B

- COUNTER AND 7-SEGMENT DECODING IN ONE PACKAGE
- EASILY INTERFACED WITH 7-SEGMENT DISPLAY TYPES
- FULLY STATIC COUNTER OPERATION: DC TO 6 MHz (TYP.) AT V_{DD} = 10V
- IDEAL FOR LOW-POWER DISPLAYS
- DISPLAY ENABLE OUTPUT - 4026B
- "RIPPLE BLANKING" AND LAMP TEST - 4033B
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATING

The **HCC 4026B/4033B** (extended temperature range) and **HCF 4026B/4033B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4026B** and **HCC/HCF 4033B** each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to a 7-segment decoded output for driving one stage in a numerical display. These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important. Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the **HCC/HCF 4026B** include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the **HCC/HCF 4033B** are RIPPLE-BLANKING INPUT AND LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT. A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. Antilock gating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (C_{out}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the **HCC/HCF 4033B**; in the **HCC/HCF 4026B** these outputs go high only when the DISPLAY ENABLE IN is high.

HCC/HCF 4026B - When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing. The CARRY OUT and UNGATED "C-SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

HCC/HCF 4033B - The **HCC/HCF 4033B** has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.07000 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the **HCC/HCF 4033B** associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the **HCC/HCF 4033B** in the next-lower significant position in the display. This procedure is continued for each succeeding **HCC/HCF 4033B** on the integer side of the display. On the fraction side of the display the RBI of the **HCC/HCF 4033B** associated with the least significant bit is connected to a low-level voltage and the RBO of that **HCC/HCF 4033B** is connected to the RBI terminal of the **HCC/HCF 4033B** in the next more-significant-bit position. Again, this procedure is continued for all **HCC/HCF 4033B's** on the fraction side of the display. In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more-significant-stage). For example: optional zero → 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the **HCC/HCF 4033B** associated with it to a high-level voltage. Ripple blanking of non-significant zeros provides an appreciable savings in display power. The **HCC/HCF 4033B** has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

HCC/HCF 4026 B
HCC/HCF 4033 B

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

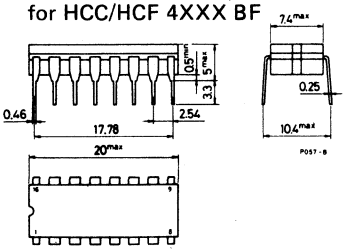
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

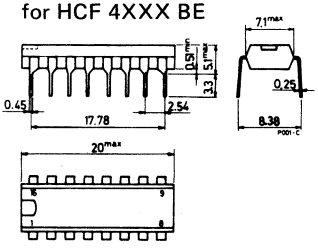
HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

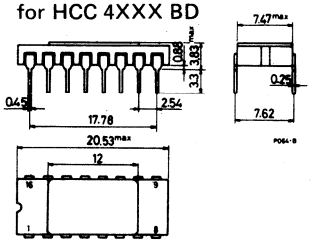
Dual in-line ceramic package for HCC/HCF 4XXX BF



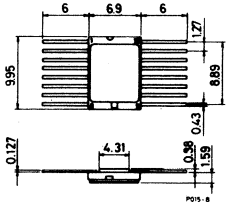
Dual in-line plastic package for HCF 4XXX BE



Dual in-line ceramic package for HCC 4XXX BD



Ceramic flat package for HCC 4XXX BK

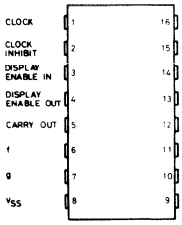


RECOMMENDED OPERATING CONDITIONS

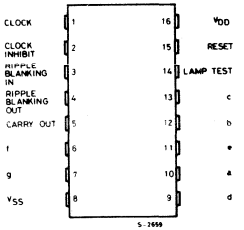
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

CONNECTION DIAGRAMS

for **4026B**

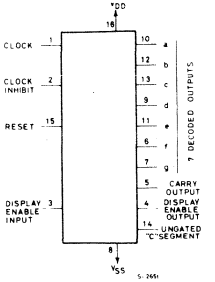


for **4033B**

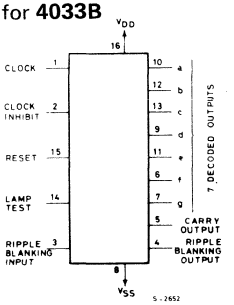


FUNCTIONAL DIAGRAMS

for **4026B**

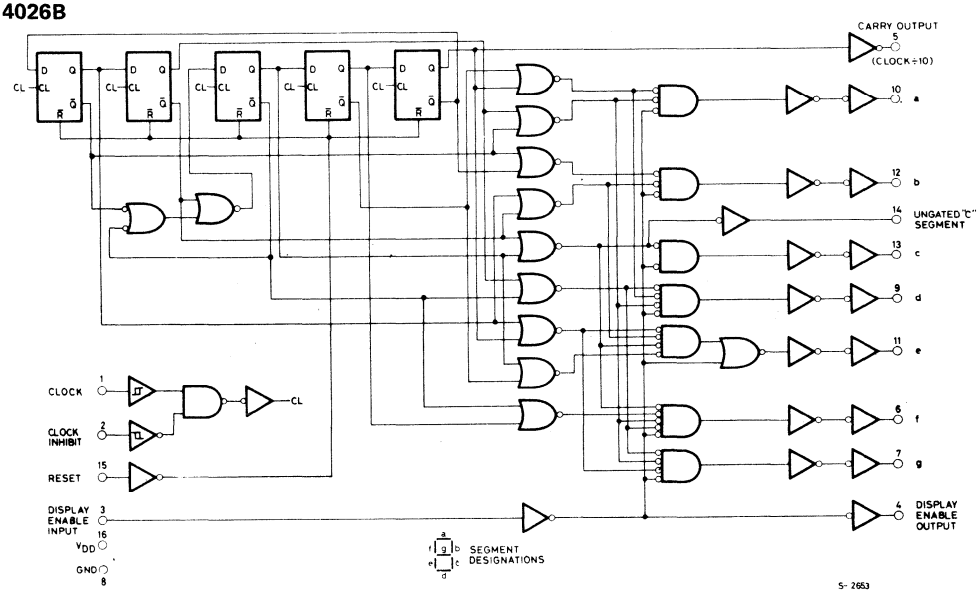


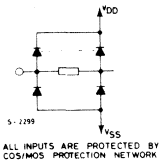
for **4033B**



LOGIC DIAGRAMS

for **4026B**

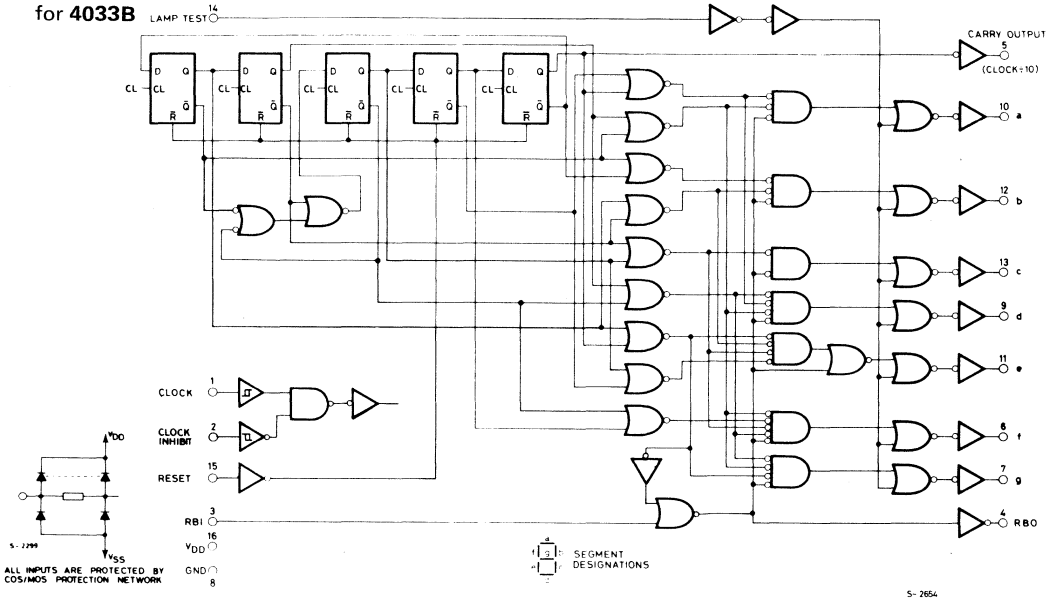




ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

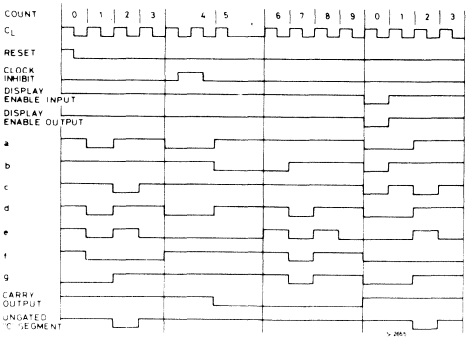
LOGIC DIAGRAMS (continued)

for **4033B**

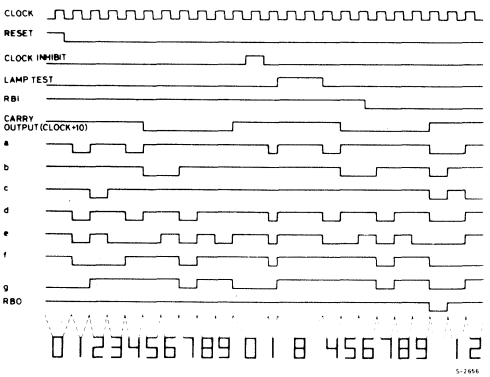


TIMING DIAGRAMS

for **4026B**



for **4033B**



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

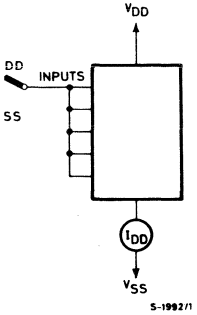
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time (Carry Out Line)	5		280		ns
		10		125		
		15		90		
t_{PLH}, t_{PHL}	Propagation delay time (Decode Out Lines)	5		475		ns
		10		220		
		15		160		
t_{THL}, t_{TLH}	Transition time (Carry Out Line)	5		100		ns
		10		50		
		15		40		
f_{CL}*	Maximum clock input frequency	5		3		MHz
		10		6		
		15		7.5		
t_{WC}	Clock pulse width	5		150		ns
		10		70		
		15		50		
t_r, t_f	Clock input rise or fall time	5	Unlimited			μs
		10				
		15				
t_{setup}	Data setup time clock inhibit	5		60		ns
		10		30		
		15		20		
RESET OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time (Carry Out Line)	5		250		ns
		10		120		
		15		85		
t_{PLH}, t_{PHL}	Propagation delay time (Decode Out Lines)	5		450		ns
		10		210		
		15		150		
t_{WR}	Reset pulse width	5		200		ns
		10		100		
		15		80		
t_R	Reset removal time	5		150		ns
		10		70		
		15		50		

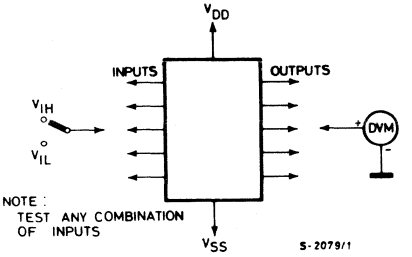
* Measured with respect to carry output line.

TEST CIRCUITS

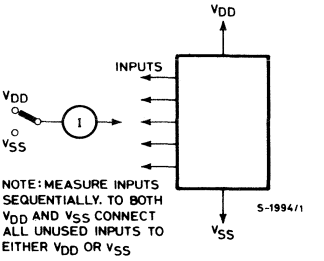
Quiescent device current



Input voltage

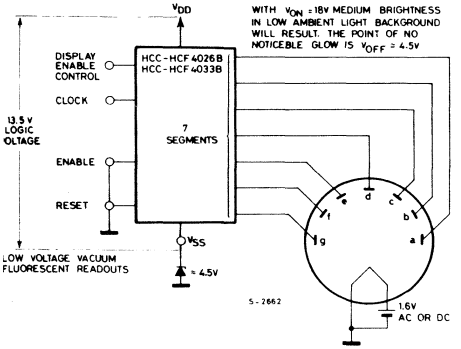


Input current

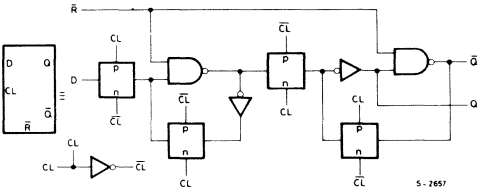


TYPICAL APPLICATIONS

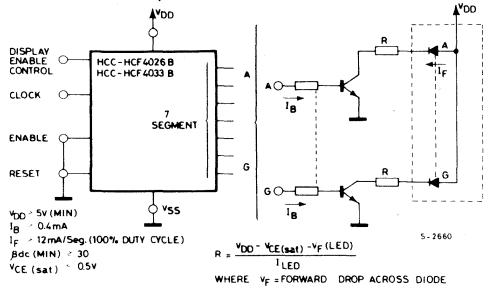
Interfacing with filament fluorescent display



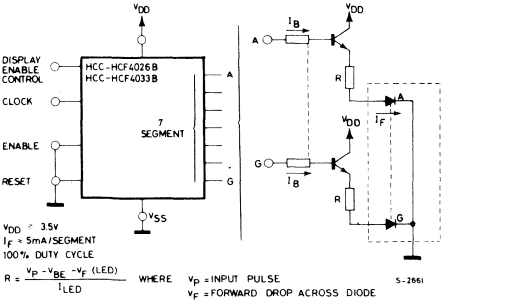
Detail of typical flip-flop stage for both types



Interfacing with LED displays (display common anode)

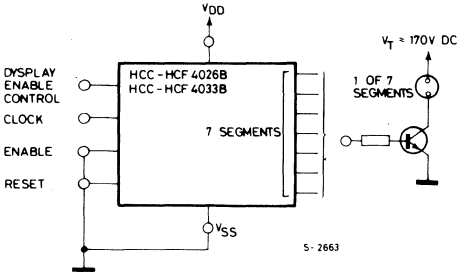


(display common cathode)

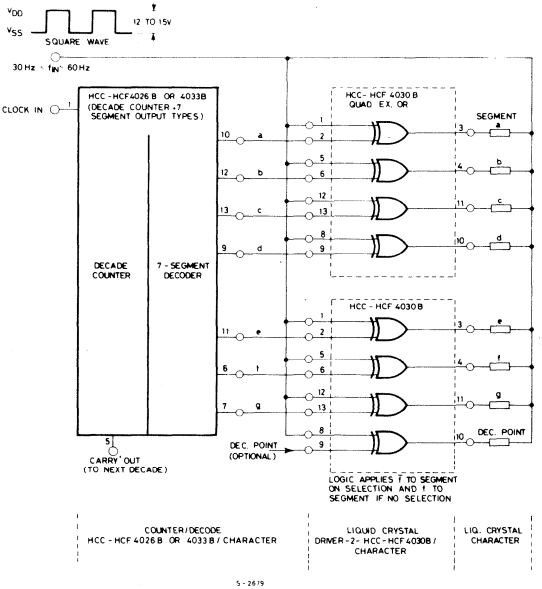


TYPICAL APPLICATION (continued)

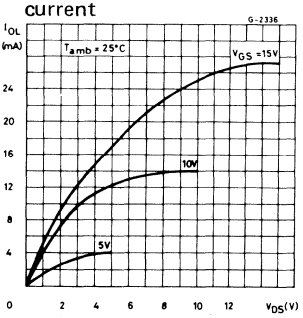
Interfacing with NIXIE tube



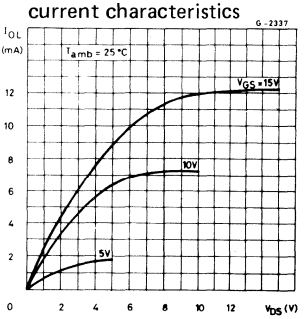
Interfacing with Liquid Cristal displays



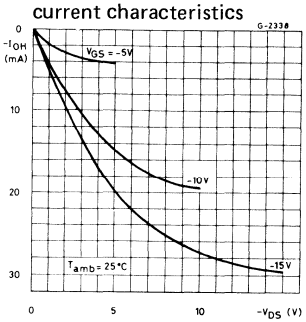
Typical output low (sink) current



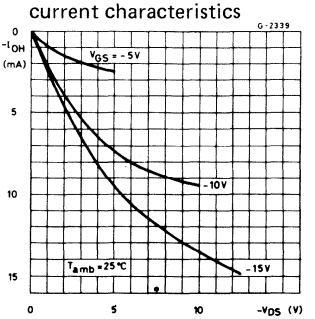
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics



Minimum output high (source) current characteristics



COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4027B

PRELIMINARY DATA

DUAL J-K MASTER-SLAVE FLIP-FLOP

- SET-RESET CAPABILITY
- STATIC FLIP-FLOP OPERATION - RETAINS STATE INDEFINITELY WITH CLOCK LEVEL EITHER "HIGH" OR "LOW"
- MEDIUM SPEED OPERATION -16 MHz (TYP.) CLOCK TOGGLE RATE AT 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE TEMPERATURE RANGE)

The **HCC 4027B** (extended temperature range) and **HCF 4027B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4027B** is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals, Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the **HCC/HCF 4013B** dual D-type flip-flop.
The **HCC/HCF 4027B** is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

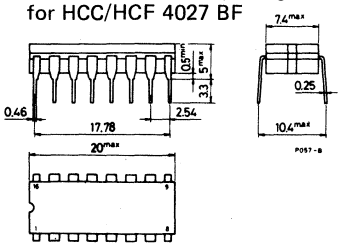
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

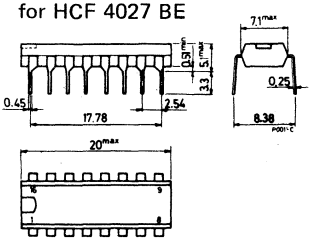
HCC 4027 BD for dual in-line ceramic package
HCC 4027 BF for dual in-line ceramic package, frit seal
HCC 4027 BK for ceramic flat package
HCF 4027 BE for dual in-line plastic package
HCF 4027 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

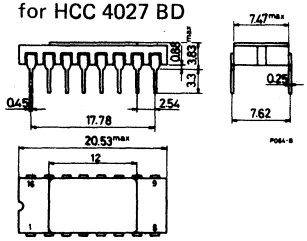
Dual in-line ceramic package for HCC/HCF 4027 BF



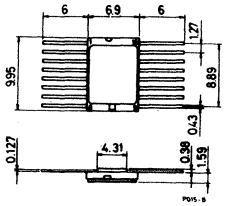
Dual in-line plastic package for HCF 4027 BE



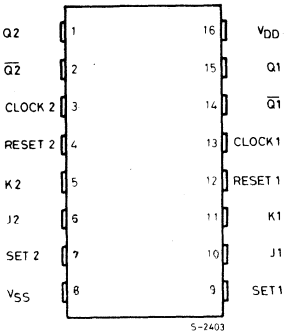
Dual in-line ceramic package for HCC 4027 BD



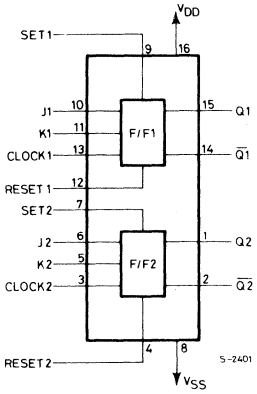
Ceramic flat package for HCC 4027 BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

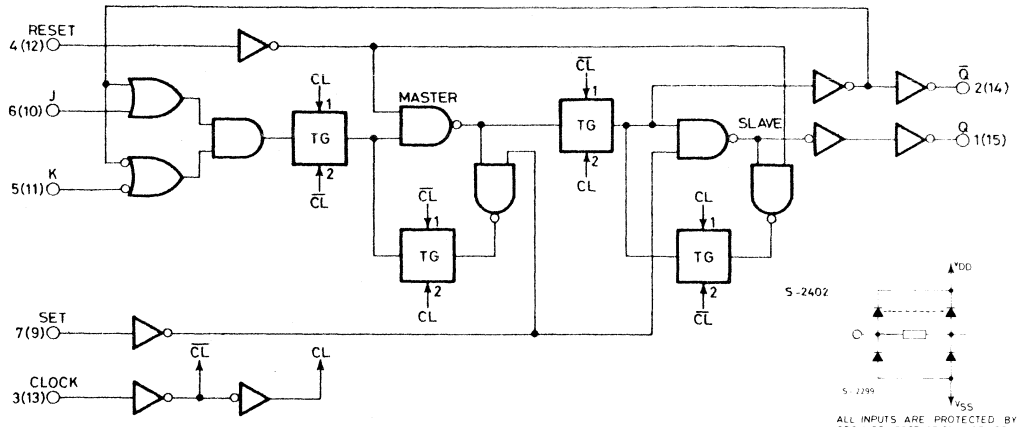


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM

One of two identical J-K flip-flops



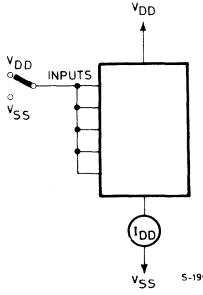
TRUTH TABLE

PRESENT STATE					CL▲	NEXT STATE		
INPUTS				OUTPUT		OUTPUTS		
J	K	S	R	Q		Q	$\bar{Q}$	
1	X	0	0	0	↑	1	0	
X	0	0	0	1	↑	1	0	
0	X	0	0	0	↑	0	1	
X	1	0	0	1	↑	0	1	
X	X	0	0	X	↓			← NO CHANGE
X	X	1	0	X	X	1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	1	1	

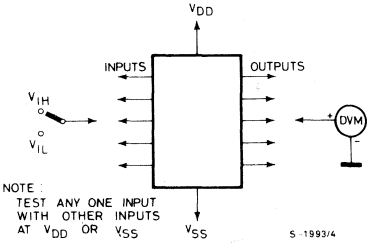
LOGIC 1 = HIGH LEVEL
LOGIC 0 = LOW LEVEL
▲ - LEVEL CHANGE
X - DON'T CARE

TEST CIRCUITS

Quiescent device current

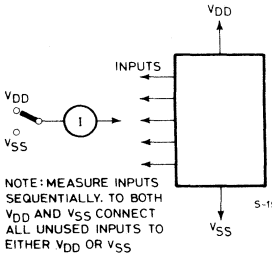


Input voltage



NOTE: TEST ANY ONE INPUT WITH OTHER INPUTS AT V_{DD} OR V_{SS}

Input leakage current



NOTE: MEASURE INPUTS SEQUENTIALLY. TO BOTH V_{DD} AND V_{SS} CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}

STATIC ELECTRICAL CHARACTERISTICS (under recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

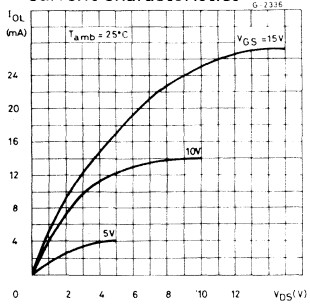
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

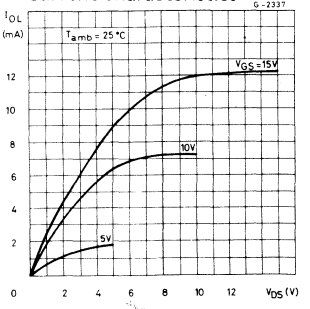
Parameter			Test conditions	Values			Unit
			V_{DD}(V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time	Clock to Q or $\overline{Q}$ outputs	5		150	300	
			10		65	130	
			15		45	90	
t_{PLH}	Propagation delay time	Set to Q or Reset to $\overline{Q}$	5		150	300	
			10		65	130	
			15		45	90	ns
t_{PHL}	Propagation delay time	Set to $\overline{Q}$ or Reset to Q	5		200	400	
			10		85	170	
			15		60	120	
t_{THL}, t_{TLH}	Transition time		5		100	200	
			10		50	100	ns
			15		40	80	
t_W	Pulse width	Clock	5	140	70		
			10	60	30		
			15	40	20		ns
t_W	Pulse width	Set or Reset	5	180	90		
			10	80	40		
			15	50	25		
t_r, t_f	Clock input rise or fall time		5			15	
			10			4	μs
			15			1	
t_{setup}	Setup time	Data	5	200	100		
			10	75	35		ns
			15	50	25		
f_{max}	Maximum clock input frequency*	Toggle Mode	5	3.5	7		
			10	8	16		MHz
			15	12	24		

* Input t_r, t_f = 5 ns.

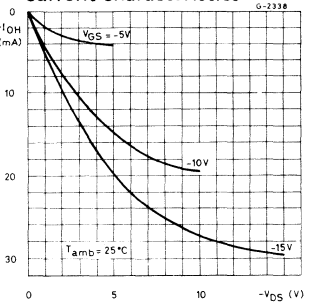
Typical output low (sink) current characteristics



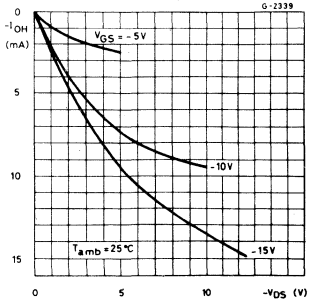
Minimum output low (sink) current characteristics



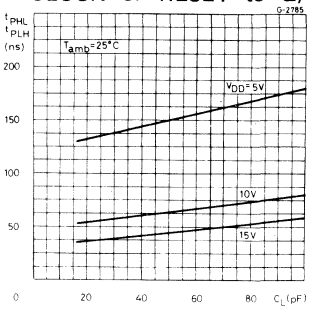
Typical output high (source) current characteristics



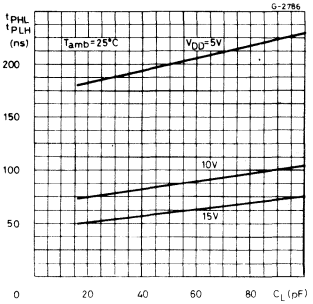
Minimum output high (source) current characteristics



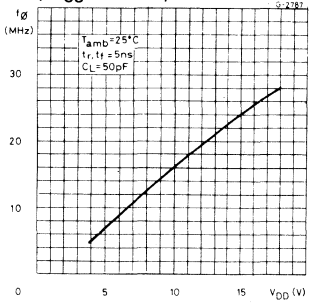
Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to $\overline{Q}$)



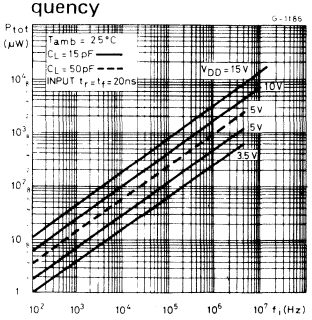
Typical propagation delay time vs. load capacitance (SET to $\overline{Q}$ or RESET to Q)



Typical maximum clock frequency vs. supply voltage (toggle mode)



Typical dynamic power dissipation/per device vs. frequency



COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4028B

PRELIMINARY DATA

BCD-TO-DECIMAL DECODER

- BCD-TO-DECIMAL DECODING OR BINARY-TO-OCTAL DECODING
- HIGH DECODED OUTPUT DRIVE CAPABILITY
- "POSITIVE LOGIC" INPUTS AND OUTPUTS: DECODED OUTPUTS GO HIGH ON SELECTION
- MEDIUM-SPEED OPERATION: t_{PHL}, t_{PLH} = 80 ns (TYP.) @ V_{DD} = 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4028B** (extended temperature range) and **HCF 4028B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.

The **HCC/HCF 4028B** types are BCD-to-decimal or binary-to-octal decoders consisting of buffering on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7 if D = "0". High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

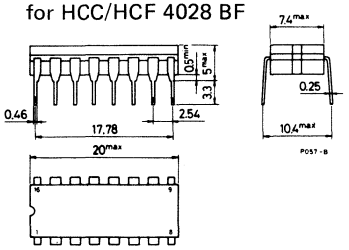
ORDERING NUMBERS:

HCC 4028 BD for dual in-line ceramic package
HCC 4028 BF for dual in-line ceramic package, frit seal
HCC 4028 BK for ceramic flat package
HCF 4028 BE for dual in-line plastic package
HCF 4028 BF for dual in-line ceramic package, frit seal

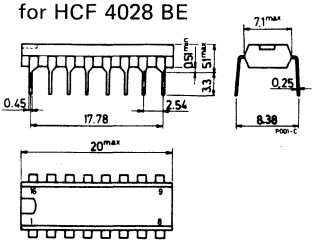
HCC/HCF 4028B

MECHANICAL DATA (dimensions in mm)

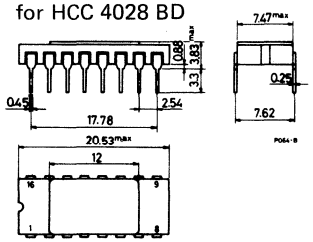
Dual in-line ceramic package
for HCC/HCF 4028 BF



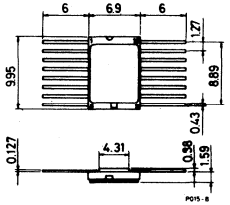
Dual in-line plastic package
for HCF 4028 BE



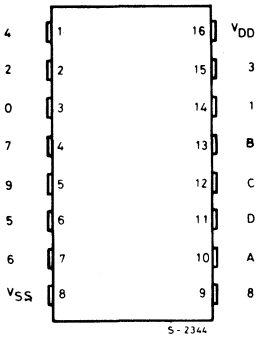
Dual in-line ceramic package
for HCC 4028 BD



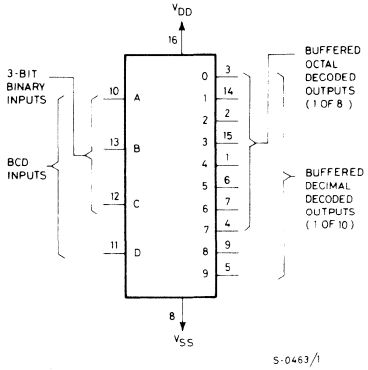
Ceramic flat package
for HCC 4028 BK



CONNECTION DIAGRAM



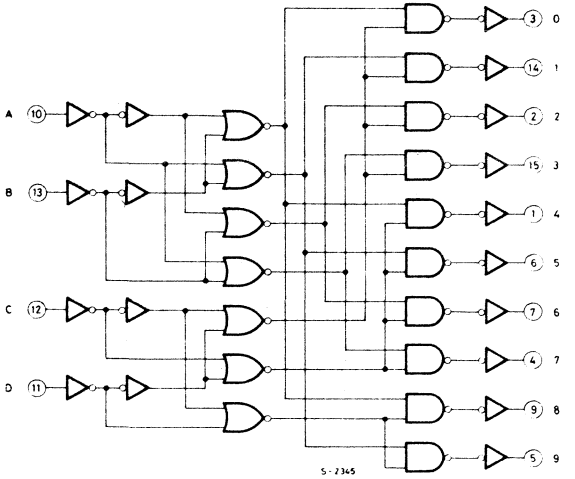
FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

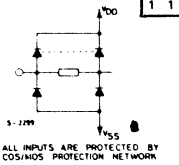
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM AND TRUTH TABLE



D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

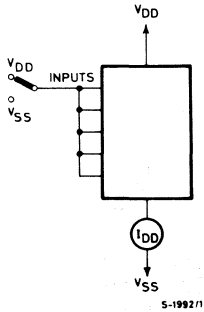
WHERE 1 = HIGH LEVEL
0 = LOW LEVEL



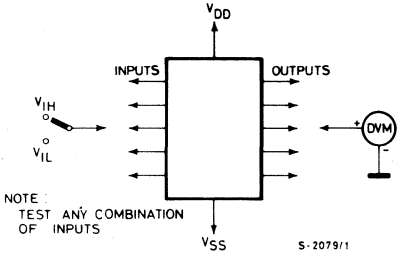
ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

TEST CIRCUITS

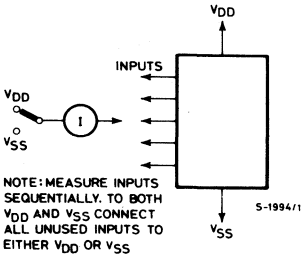
Quiescent device current



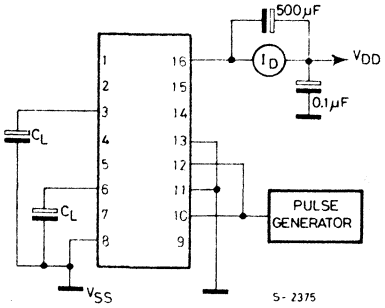
Noise immunity



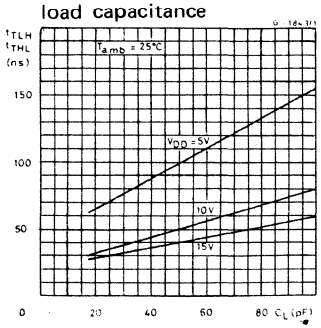
Input leakage current



Dynamic power dissipation



Typical transition time vs. load capacitance



STATIC ELECTRICAL CHARACTERISTICS (under recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		± 0.1		± 10^{-5}	± 0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

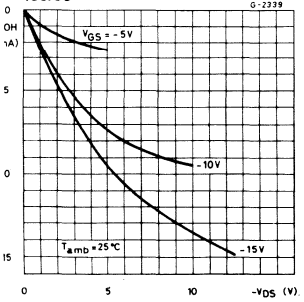
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

**Any input

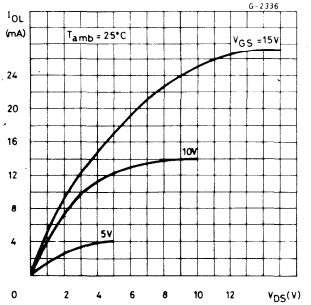
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
	V_{DD}(V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH} Propagation delay time (Clock to "Out")	5		175	350	ns
	10		80	160	
	15		60	120	
t_{THL}, t_{TLH} Transition time	5		100	200	ns
	10		50	100	
	15		40	80	

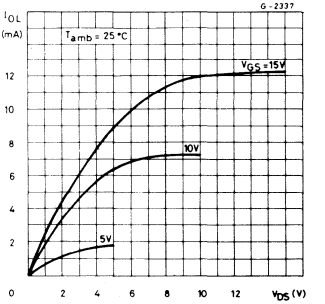
Minimum output high (source) current characteristics



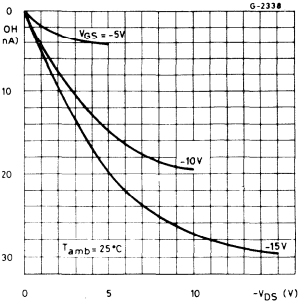
Typical output low (sink) current



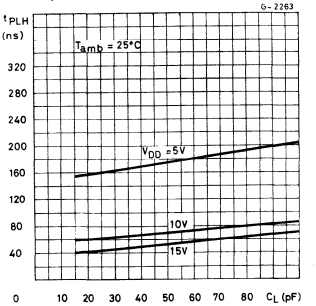
Minimum output low (sink) current characteristics



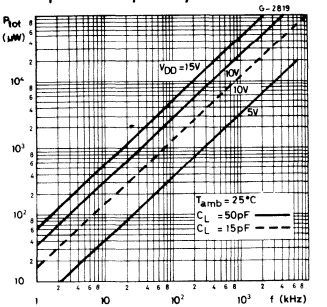
Typical output high (source) current characteristics



Typical propagation delay time as a function of load capacitance



Typical dynamic power dissipation as a function of input frequency



TYPICAL APPLICATIONS

The circuit shown in fig. 1 converts any 4-bit code to a decimal or hexadecimal code. Fig. 2 shows a number of codes and the decimal or hexadecimal number in these codes which must be applied to the input pins of the HCC/HCF 4028B to select a particular output. For example: in order to get a "high" on output n. 8 the input must be either an 8 expressed in 4-bit binary code, a 15 expressed in 4-bit Gray code, or a 5 expressed in Excess-3 code.

Fig. 1 - Code conversion circuit

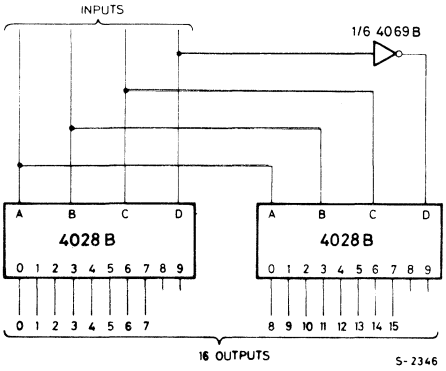


Fig. 2 - Code conversion chart

INPUTS				INPUT CODES						OUTPUT NUMBER																
				Hexa Decimal		Decimal																				
D	C	B	A	4 BIT BINARY	4 BIT GRAY	EXCESS 3	EXCESS 3 GRAY	AIKEN	4 2 2 1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0			0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1			1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	2	3		0	2	2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	3	2	0	1	3		0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	4	7	1	4	4		0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	5	6	2			3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	6	4	3	1		4	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	7	5	4	2			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	8	15	5				0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	9	14	6			5	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	10	12	7	9		6	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	11	13	8		5		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	12	8	9	5	6		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	13	9		6	7	7	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	14	11		8	8	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	15	10		7	9	9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Fig. 3 - 6-bit binary to 1 of 64 address decoder

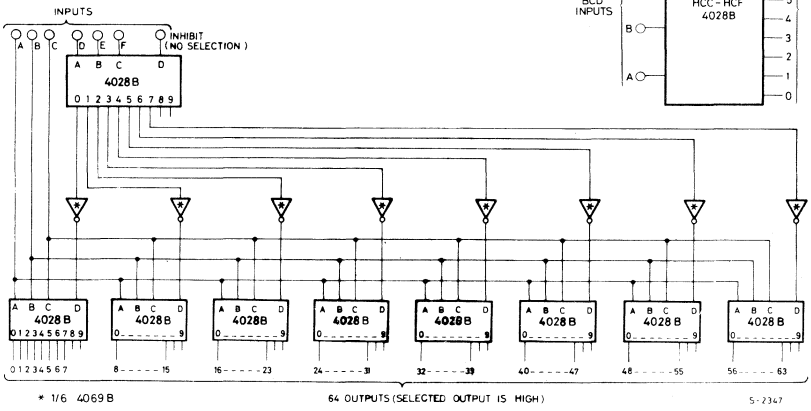
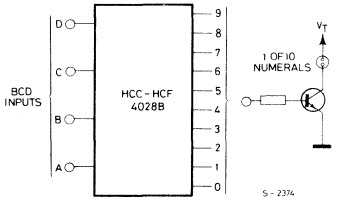


Fig. 4 - Neon readout (Nixie Tube) display application



COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4029B

PRELIMINARY DATA

PRESETTABLE UP/DOWN COUNTER BINARY OR BCD-DECADE

- MEDIUM SPEED OPERATION - 8 MHz (TYP.) @ C_L = 50 pF AND V_{DD}-V_{SS} = 10V
- MULTI-PACKAGE PARALLEL CLOCKING FOR SYNCHRONOUS HIGH SPEED OUTPUT RESPONSE OR RIPPLE CLOCKING FOR SLOW CLOCK INPUT RISE AND FALL TIMES
- "PRESET ENABLE" AND INDIVIDUAL "JAM" INPUTS PROVIDED
- BINARY OR DECADE UP/DOWN COUNTING
- BCD OUTPUTS IN DECADE MODE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4029B** (extended temperature range) and **HCF 4029B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4029B** consists of a four-stage binary or BCD-decade up/down counter with provisions for look-ahead carry in both counting modes. The inputs consist of a single CLOCK, CARRY-IN (CLOCK ENABLE), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals. Q1, Q2, Q3, Q4 and a CARRY OUT signal are provided as outputs. A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter is advanced one count at the positive transition of the clock when the CARRY-IN and PRESET ENABLE signals are low. Advancement is inhibited when the CARRY-IN or PRESET ENABLE signals are high. The CARRY-OUT signal is normally high and goes low when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY-IN signal is low. The CARRY-IN signal in the low state can thus be considered a CLOCK ENABLE. The CARRY-IN terminal must be connected to V_{SS} when not in use. Binary counting is accomplished when the BINARY/DECADE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts Up when to UP/DOWN INPUT is high, and Down when the UP/DOWN INPUT is low. Multiple packages can be connected in either a parallel-clocking or a ripple-clocking arrangement as shown in cascading counter packages. Parallel clocking provides synchronous control and hence faster response from all counting outputs. Ripple-clocking allows for longer clock input rise and fall times.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

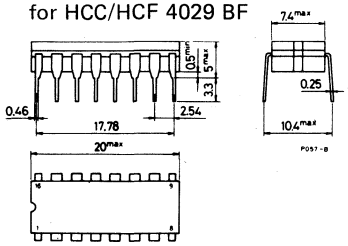
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

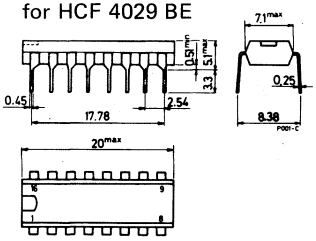
HCC 4029 BD for dual in-line ceramic package
HCC 4029 BF for dual in-line ceramic package, frit seal
HCC 4029 BK for ceramic flat package
HCF 4029 BE for dual in-line plastic package
HCF 4029 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

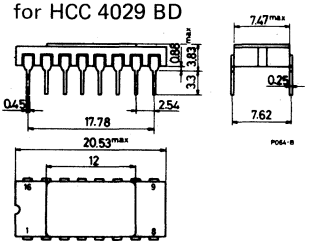
Dual in-line ceramic package for HCC/HCF 4029 BF



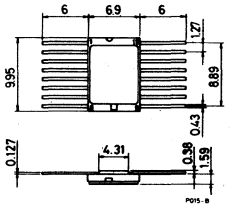
Dual in-line plastic package for HCF 4029 BE



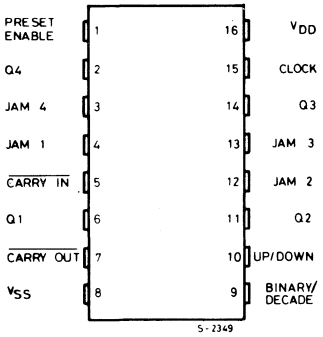
Dual in-line ceramic package for HCC 4029 BD



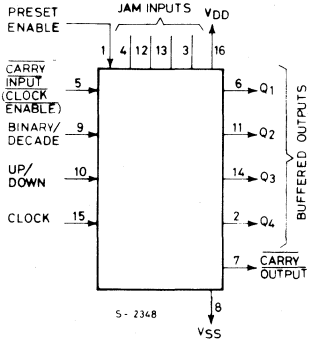
Ceramic flat package for HCC 4029 BK



CONNECTION DIAGRAM



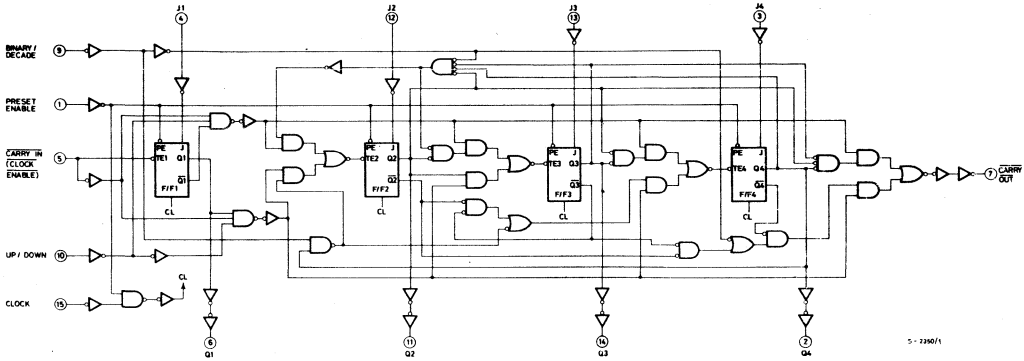
FUNCTIONAL DIAGRAM

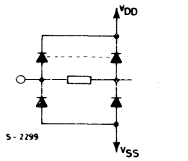


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

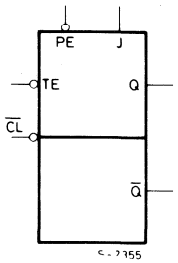
SCHEMATIC DIAGRAM





ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

TRUTH TABLES



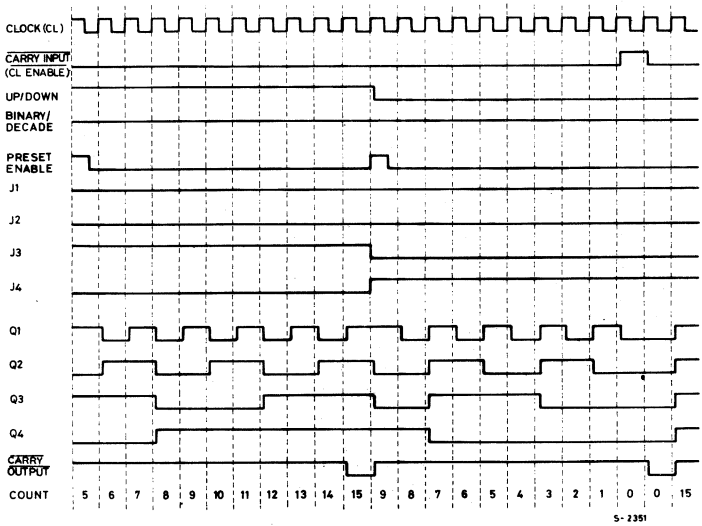
CLOCK	TE	PE	J	Q	$\overline{Q}$
X	X	0	0	0	1
⊓	0	1	X	$\overline{Q}$	Q
X	X	0	1	1	0
⊓	1	1	X	Q	$\overline{Q}$ NC
⊔	X	1	X	Q	$\overline{Q}$ NC

X = DON'T CARE

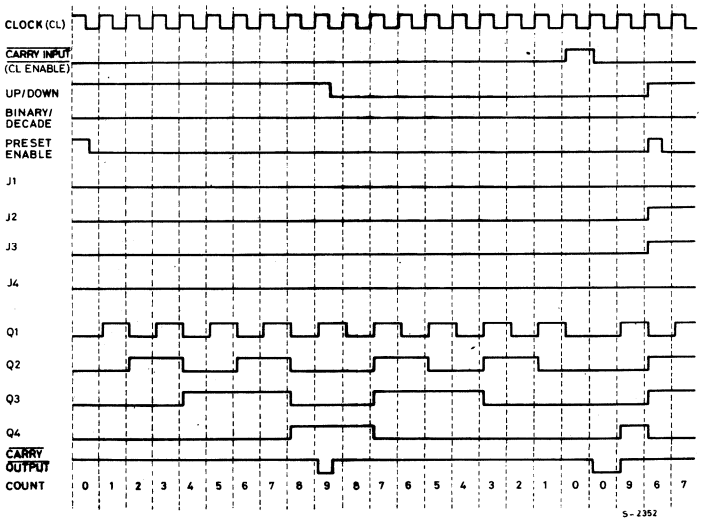
CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC. (B/D)	1	BINARY COUNT
	0	DECADE COUNT
UP/DOWN (U/D)	1	UP COUNT
	0	DOWN COUNT
PRESET ENABLE (PE)	1	JAM IN
	0	NO JAM
$\overline{\text{CARRY IN}}$ ($\overline{\text{CI}}$) $\overline{\text{(CLOCK ENABLE)}}$	1	NO COUNTER ADVANCE AT POS. CLOCK TRANSITION
	0	ADVANCE COUNTER. AT POS. CLOCK TRANSITION

TIMING DIAGRAMS

Binary mode



Decade mode



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

** Any input

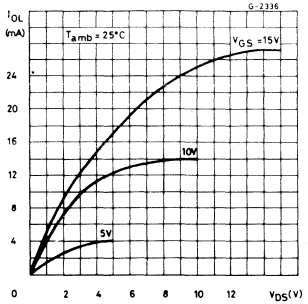
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION						
t_{PLH}, t_{PHL}	Propagation delay time (Q outputs)	5		165		ns
		10		75		
		15		55		
t_{PLH}, t_{PHL}	Propagation delay time (Carry output)	5		280		ns
		10		130		
		15		95		
t_{TLH}, t_{THL}	Transition time (Q outputs, carry output)	5		100		ns
		10		50		
		15		40		
t_W	Minimum clock pulse width	5		60		ns
		10		30		
		15		24		
t_r, t_f**	Clock rise and fall time	5				μs
		10		> 200		
		15				
t_{setup}*	Minimum setup time (Carry input)	5		30		ns
		10		10		
		15		6		
t_{setup}	Minimum setup time (B/D or UD)	5		150		
		10		70		
		15		50		
f_{max}	Maximum clock input frequency	5		4.6		MHz
		10		10		
		15		14		
PRESET ENABLE						
t_{PHL}, t_{PLH}	Propagation delay time (Q outputs)	5		200		ns
		10		90		
		15		65		
t_{PHL}, t_{PLH}	Propagation delay time (Carry output)	5		320		
		10		145		
		15		105		
t_W	Minimum preset enable (pulse width)	5		50		ns
		10		35		
		15		25		
t_{rem}*	Minimum preset enable (removal time)	5		120		ns
		10		55		
		15		40		
CARRY INPUT						
t_{PHL}, t_{PLH}	Propagation delay time (Carry output)	5		140		ns
		10		70		
		15		50		

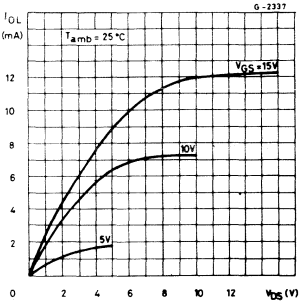
* From Up/Down, Binary/Decode, Carry-In, or Preset Enable Control Inputs to Clock Edge.

** If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the carry output driving stage for the estimated capacitive load.

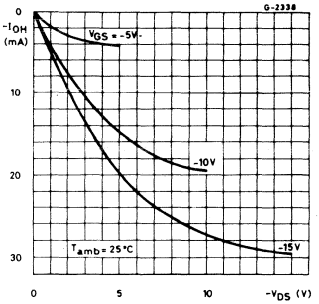
Typical output low (sink) current characteristics



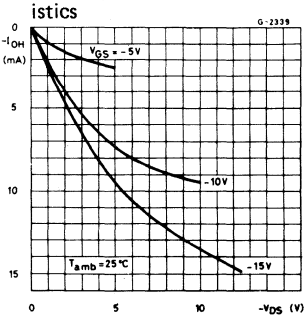
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics

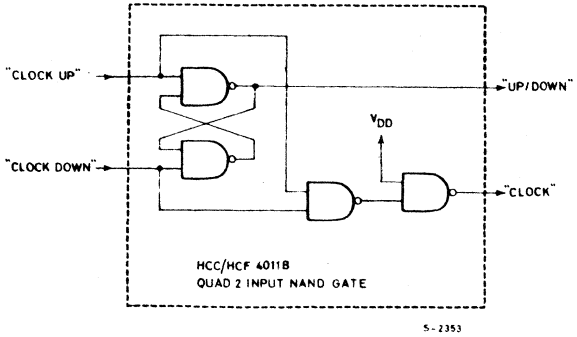


Minimum output high (source) current characteristics



APPLICATIONS

Conversion of clock up, clock down input signals to clock and up/down input signals.

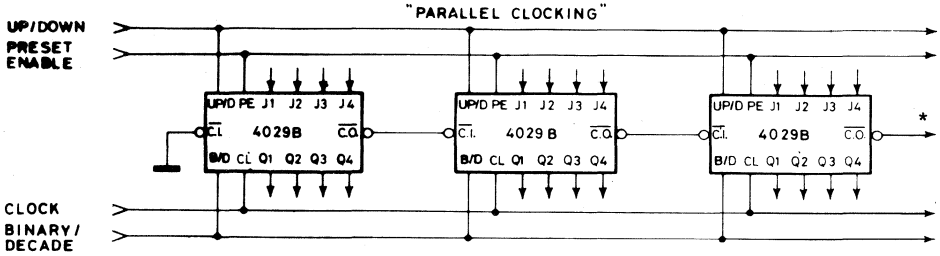


The **HCC/HCF 4029B** CLOCK and UP/DOWN inputs are used directly in most applications. In applications where CLOCK UP and CLOCK DOWN inputs are provided, conversion to the **HCC/HCF 4029B** CLOCK and UP/DOWN inputs can easily be realized by use of the circuit.

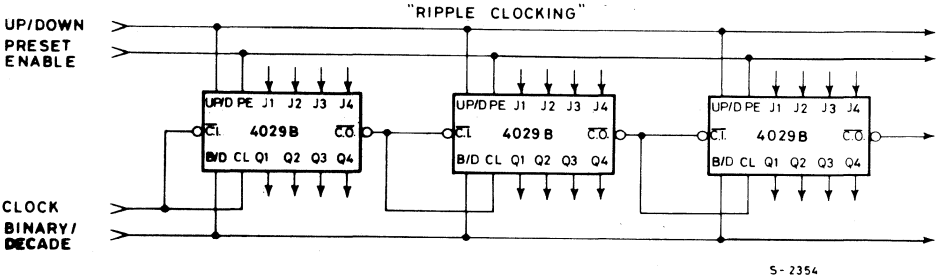
HCC/HCF 4029B changes count on positive transitions of CLOCK UP or CLOCK DOWN inputs. For the gate configuration shown below, when counting up the CLOCK DOWN input must be maintained high and conversely when couting down the CLOCK UP input must be maintained high.

APPLICATIONS (continued)

Cascading counter packages



* CARRY-OUT lines at the 2nd, 3rd, et., stages may have a negative-going glitch pulse resulting from differential delays of different **HCC/HCF 4029B** IC's. These negative-going glitches do not affect proper **HCC/HCF 4029B** operation, However, if the CARRY-OUT signals are used to trigger other edge-sensitive logic devices, such as FF's or counters, the CARRY-OUT signals should be gated with the clock signal using a 2-input NOR gate such as **HCC/HCF 4001B.**



Ripple Clocking Mode:
The Up/Down control can be changed at any count. The only restriction on changing the Up/Down control is that the clock input to the first counting stage must be high.

COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

QUAD EXCLUSIVE - OR GATE

- MEDIUM-SPEED OPERATION - $t_{PHL} = t_{PLH} = 60$ ns (TYP.) @ $C_L = 50$ pF and $V_{DD}-V_{SS} = 10V$
- LOW OUTPUT IMPEDANCE: 500Ω (TYP.) @ $V_{DD}-V_{SS} = 10V$
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4030B** (extended temperature range) and **HCF 4030B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4030B** types consist of four independent Exclusive-OR gates integrated on a single monolithic silicon chip. Each Exclusive-OR gate consists of four n-channel and four p-channel enhancement-type transistors. All inputs and outputs are protected against electrostatic effects.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

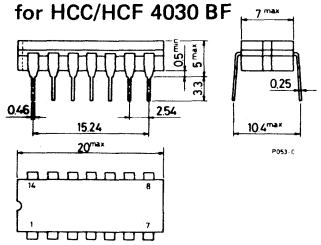
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

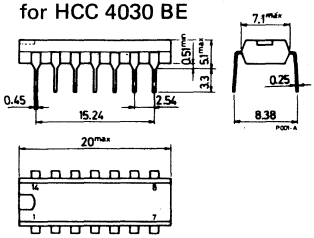
HCC 4030 BD	for dual in-line ceramic package
HCC 4030 BF	for dual in-line ceramic package, frit seal
HCC 4030 BK	for ceramic flat package
HCF 4030 BE	for dual in-line plastic package
HCF 4030 BF	for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

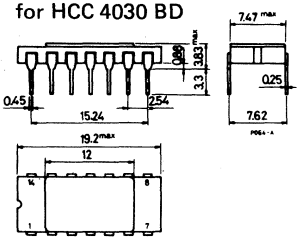
Dual in-line ceramic package for HCC/HCF 4030 BF



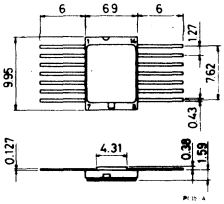
Dual in-line plastic package for HCC 4030 BE



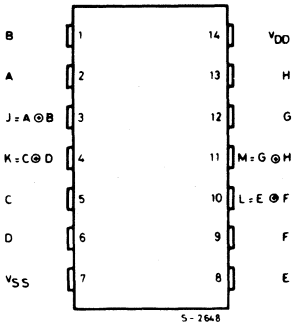
Dual in-line ceramic package for HCC 4030 BD



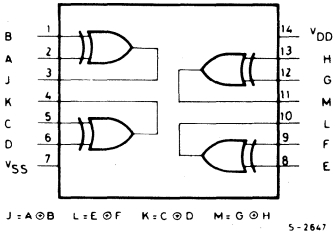
Ceramic flat package for HCC 4030 BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

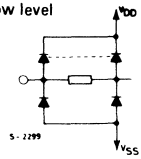


TRUTH TABLE

One of four identical gates

A	B	J
0	0	0
1	0	1
0	1	1
1	0	0

Where "1" = High level
"0" = Low level



ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

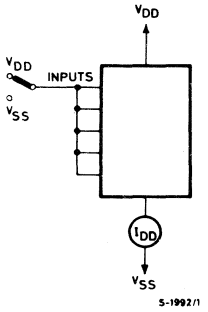
STATIC ELECTRICAL CHARACTERISTICS (under recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

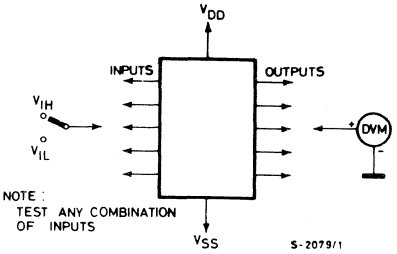
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

TEST CIRCUITS

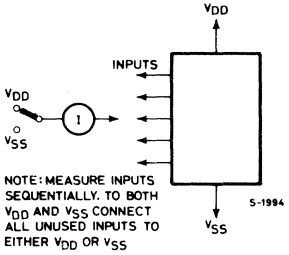
Quiescent device current



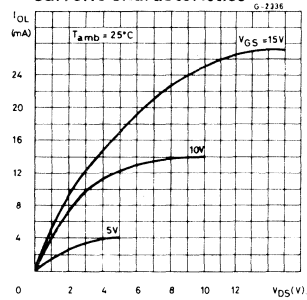
Input voltage



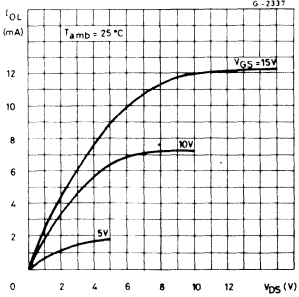
Input leakage current



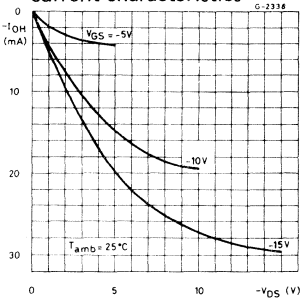
Typical output low (sink) current characteristics



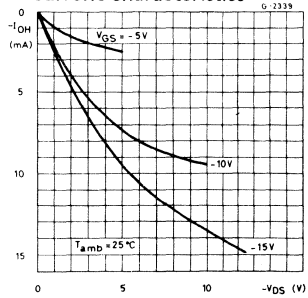
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics



Minimum output high (source) current characteristics

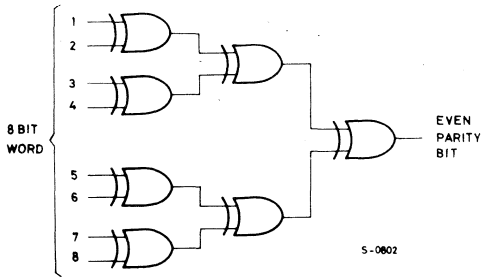


DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

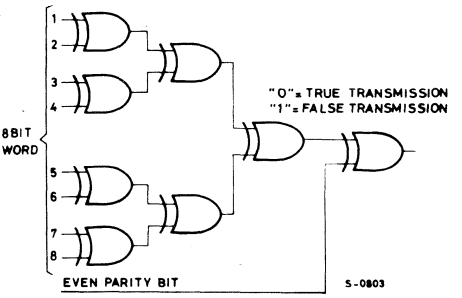
Parameter	Test conditions	Values			Unit
	V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time	5		150		ns
	10		60		
	15		45		
t_{TLH}, t_{THL} Transition time	5		100		ns
	10		50		
	15		40		

TYPICAL APPLICATIONS

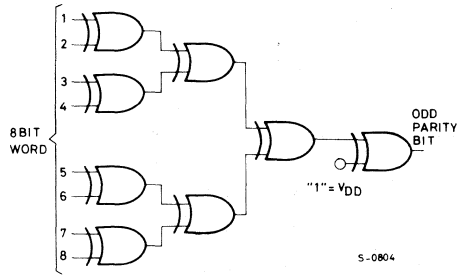
Even-parity-bit generator
(1-3/4 x **HCC/HCF 4030B**)



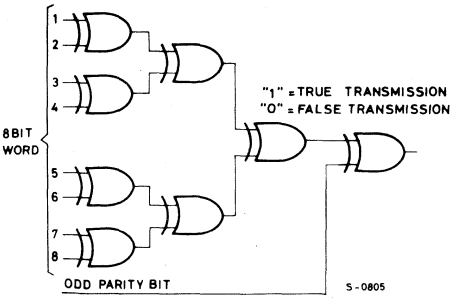
Even-parity checker
(2 x **HCC/HCF 4030B**)



Odd-parity-bit generator
(2 x **HCC/HCF 4030B**)

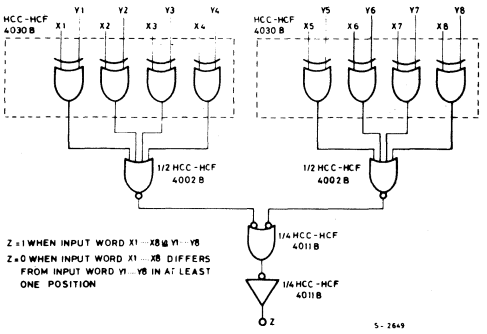


Odd-parity checker
(2 x **HCC/HCF 4030B**)



TYPICAL APPLICATIONS (continued)

8-bit comparator



8-bit two's complement adder-substractor

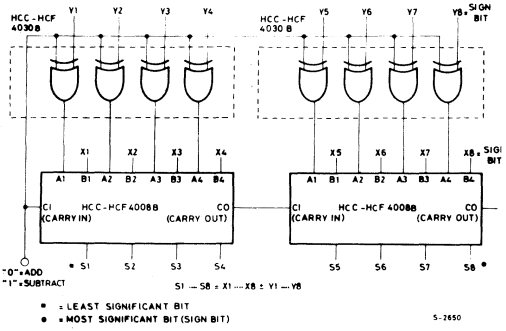


TABLE 1

Two's complement numbers and their equivalent decimal values

X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1			X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	
0	0	0	0	0	0	0	0	=	0	1	1	1	1	1	1	1	1	= -1
0	0	0	0	0	0	0	1	=	1	1	1	1	1	1	1	1	0	= -2
0	0	0	0	0	0	1	0	=	2	1	1	1	1	1	1	0	1	= -3
0	0	0	0	0	0	1	1	=	3	1	1	1	1	1	1	0	0	= -4
										1	1	1	1	1	0	1	1	= -5
0	1	1	1	1	1	1	0	=	126	1	0	0	0	0	0	0	1	= -127
0	1	1	1	1	1	1	1	=	127	1	0	0	0	0	0	0	0	= -128

The two's complement adder-substractor can add or substract any two of the numbers in TABLE 1. For example

a)

		SIGN BIT								
+	=									
-5	X	0	0	0	0	0	1	0		2 +
—	Y	1	1	1	1	1	0	1	1	-5 +
	CI								0	
	S	0	1	1	1	1	1	1	0	1 = -3
	CO									

b)

		SIGN BIT								
- 2	=									
	X	1	1	1	1	1	1	1	0	- 2 +
- 5	Y	1	1	1	1	1	0	1	1	- 5
	$\bar{Y}$	0	0	0	0	0	1	0	0	+
	CI								1	
	S	1	0	0	0	0	0	1	1	= 3
	CO									

COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

64-STAGE STATIC SHIFT REGISTER

- FULLY STATIC OPERATION: DC TO 16 MHz (TYP.) @ V_{DD}-V_{SS}= 15V
- STANDARD TTL DRIVE CAPABILITY ON Q OUTPUT
- RECIRCULATION CAPABILITY
- THREE CASCADING MODES: DIRECT CLOCKING FOR HIGH-SPEED OPERATION
  DELAYED CLOCKING FOR REDUCED CLOCK DRIVE REQUIREMENTS
  ADDITIONAL 1/2 STAGE FOR SLOW CLOCKS
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4031B** (extended temperature range) and **HCF 4031B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.

The **HCC/HCF 4031B** is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage). The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 16 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The **HCC/HCF 4031B** has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output, like the delayed clock CL_D, is used with clocks having slow rise and fall times.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

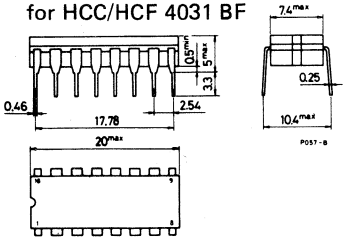
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

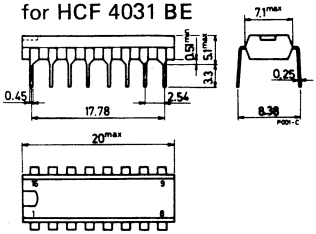
HCC 4031 BD for dual in-line ceramic package
HCC 4031 BF for dual in-line ceramic package, frit seal
HCC 4031 BK for ceramic flat package
HCF 4031 BE for dual in-line plastic package
HCF 4031 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

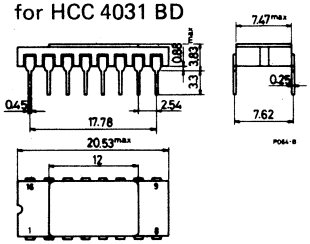
Dual in-line ceramic package for HCC/HCF 4031 BF



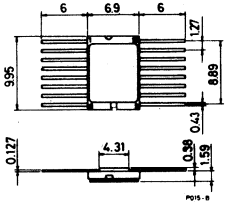
Dual in-line plastic package for HCF 4031 BE



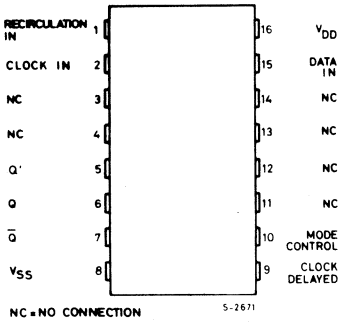
Dual in-line ceramic package for HCC 4031 BD



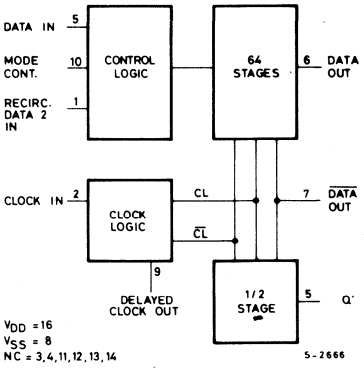
Ceramic flat package for HCC 4031 BK



CONNECTION DIAGRAM



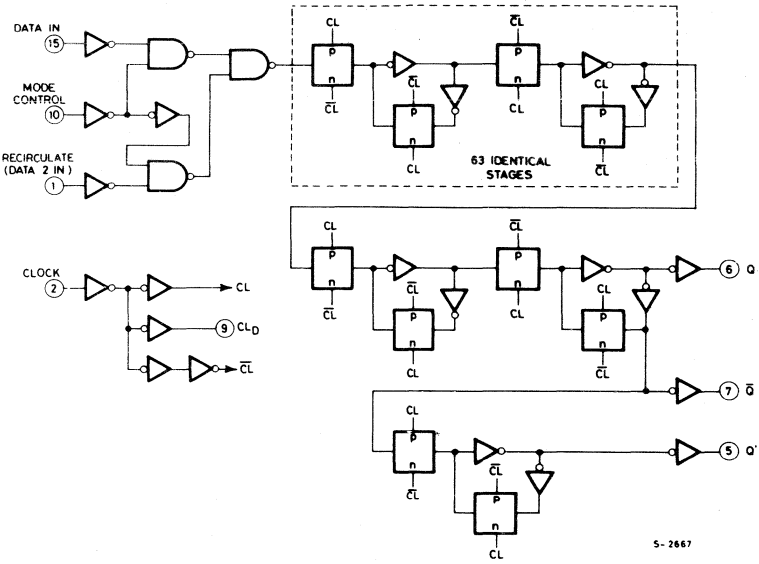
FUNCTIONAL DIAGRAM

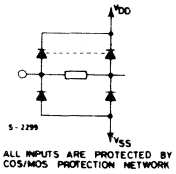


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM AND TRUTH TABLES





INPUT CONTROL CIRCUIT

DATA	RECIRC.	MODE	BIT INTO STAGE I
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

TYPICAL STAGE

Data	CL▲	Data + 1
0	⌒	0
1	⌒	1
X	⌒	NC

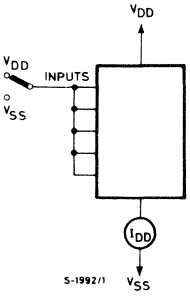
OUTPUT FROM Q' (PIN 5)

Data +63	CL▲	Data +64.5
0	⌒	0
1	⌒	1
X	⌒	NC

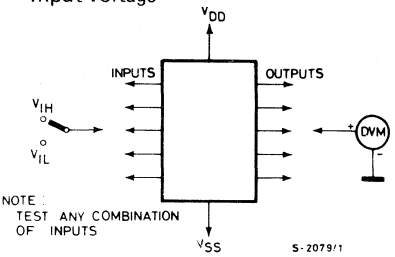
1 = HIGH LEVEL 0 = LOW LEVEL NC = NO CHANGE
X = DON'T CARE ▲ = LEVEL CHANGE

TEST CIRCUITS

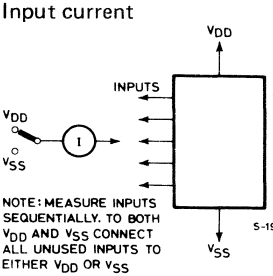
Quiescent device current



Input voltage



Input current



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	10		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output source current (Source) Q,$\overline{Q}$,Q, CL_D	HCC types	0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		mA
			0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current Q	HCC types	0/ 5	0.4		5	2.56		2.04	4		1.44		mA
			0/10	0.5		10	6.4		5.2	10.4		3.6		
			0/15	1.5		15	16.8		13.6	27.2		9.6		
		HCF types	0/ 5	0.4		5	2.44		2.04	4		1.68		
			0/10	0.5		10	6		5.2	10.4		4.4		
			0/15	1.5		15	16		13.6	27.2		11.2		
I_{OL}	Output sink current $\overline{Q}$,Q' CL_D**		0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		± 0.1		± 10^{-5}	± 0.1		± 1	μA
C_i	Input capacitance			Any input						5	7.5			pF

* T_{Low}=-55°C for **HCC** device; -40°C for **HCF** device. T_{High}=+125°C for **HCC** device; +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

** For I_{OL}, CL_D is garanted only for typical values at T_{amb}= 25°C.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time Positive Clock to Q or $\overline{Q}$ Negative Clock to Q'		5		200		ns
			10		100		
			15		80		
t_{PLH}	Propagation delay time Positive Clock to CL_D		5		100		ns
			10		50		
			15		35		
t_{THL} t_{TLH}	Transition time (Any output)		5		100		ns
			10		50		
			15		40		
t_{hold}	Data hold time		5		0		ns
			10		0		
			15		0		
t_W	Clock pulse width		5		100		
			10		45		
			15		30		
t_r, t_f	Clock input rise or fall time*		5		15		μs
			10		15		
			15		15		
t_{setup}	Data setup time		5		50		ns
			10		25		
			15		20		
f_{max}	Maximum Toggle Mode clock input frequency**		5		5		MHz
			10		12		
			15		16		

Note: * If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 50 pF and the transition time of the output driving stage.

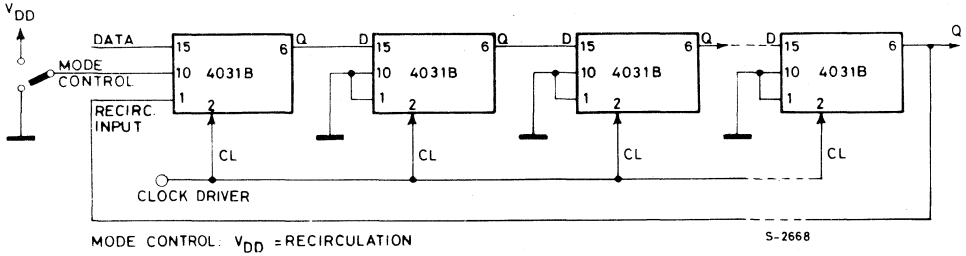
** Maximum Clock Frequency for Cascaded Units:

a) Using Delayed Clock Feature — $f_{max} = \frac{1}{(n-1)\ CL_D \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}}$ where n = number of packages

b) Not Using Delayed Clock — $f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$

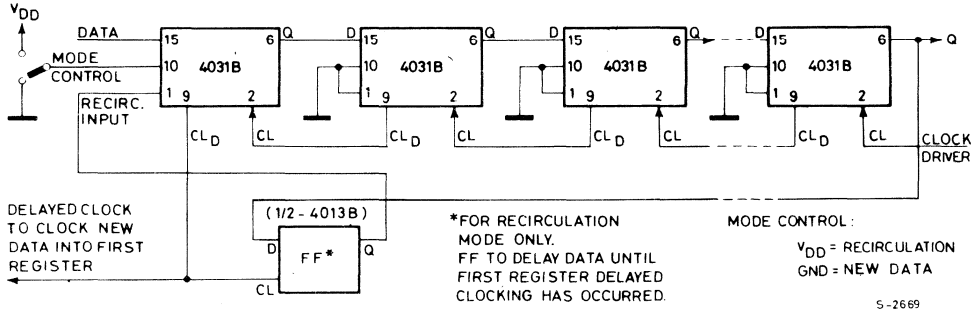
TYPICAL APPLICATIONS

Cascading using direct clocking for high speed operation
(see clock rise and fall time requirement)

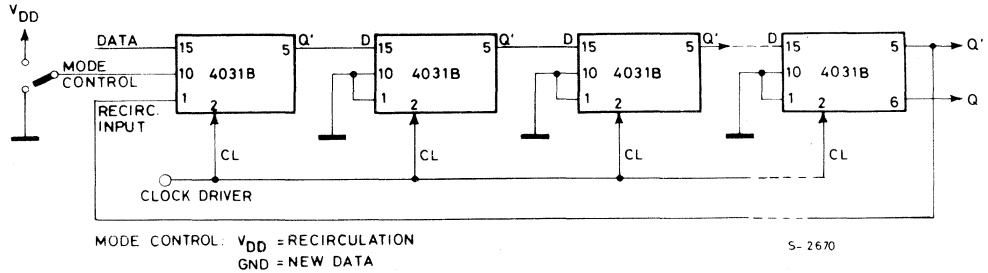


MODE CONTROL: V_{DD} = RECIRCULATION
GND = NEW DATA

Cascading using delayed clocking for reduced clock drive requirements

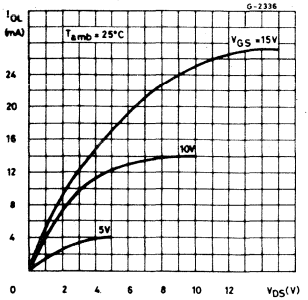


Cascading using half-clock-pulse delayed data output (Q') to permit use of slow rise and fall time clock inputs.

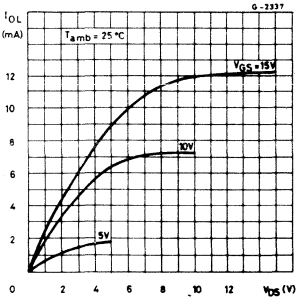


MODE CONTROL: V_{DD} = RECIRCULATION
GND = NEW DATA

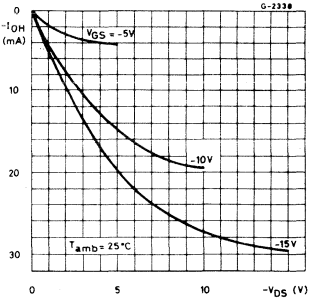
Typical output low (sink) current characteristics



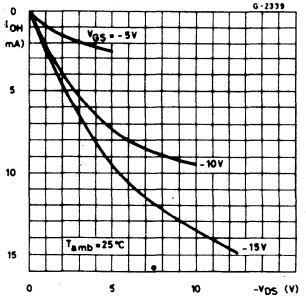
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics



Minimum output high (source) current characteristics



COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

TRIPLE SERIAL ADDERS

- INVERT INPUTS ON ALL ADDERS FOR SUM COMPLEMENTING APPLICATIONS
- FULLY STATIC OPERATION . . . . . DC TO 10 MHz (TYP.) @ V_{DD}= 10V
- BUFFERED INPUTS AND OUTPUTS
- SINGLE-PHASE CLOCKING
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATING

The **HCC/4032B/4038B** (extended temperature range) and **HCF 4032B/4038B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4032B** and **HCC/HCF 4038B** types consist of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has two provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the **HCC/HCF 4032B** or at the negative-going clock for the **HCC/HCF 4038B**, thus, for spike-free operation the input data transitions should occur as soon as possible after the triggering edge. The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one-bit-position before the application of the first bit of the next word.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

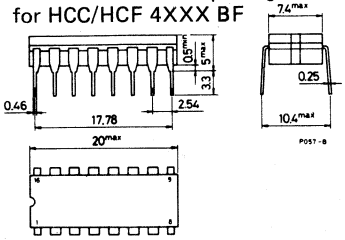
ORDERING NUMBERS:

HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

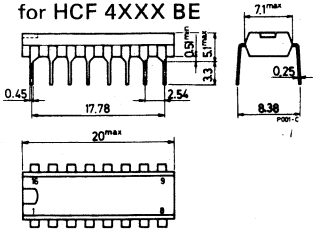
HCC/HCF 4032B
HCC/HCF 4038B

MECHANICAL DATA (dimensions in mm)

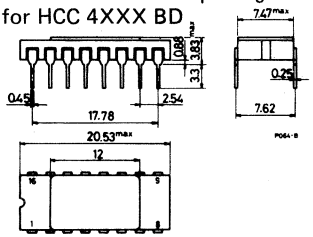
Dual in-line ceramic package
for HCC/HCF 4XXX BF



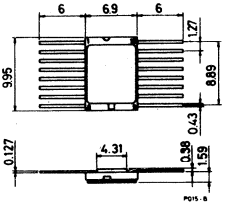
Dual in-line plastic package
for HCF 4XXX BE



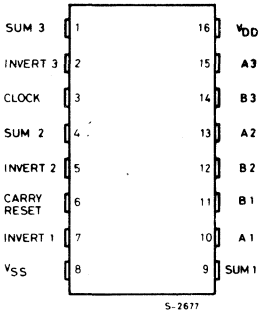
Dual in-line ceramic package
for HCC 4XXX BD



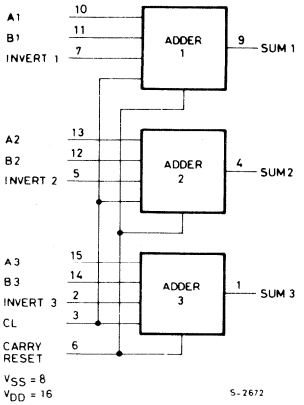
Ceramic flat package
for HCC 4XXX BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

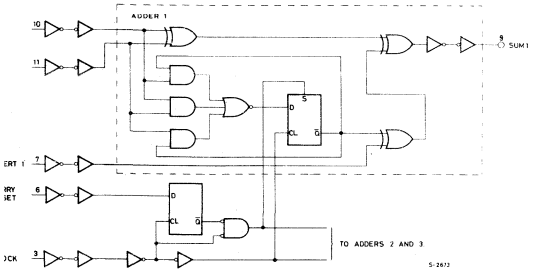


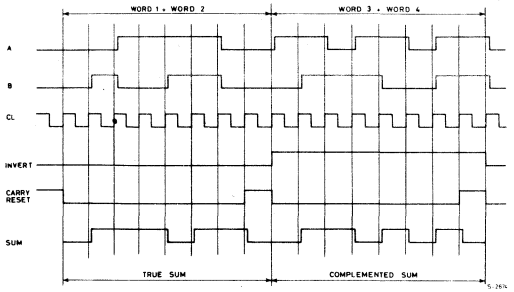
RECOMMENDED OPERATING CONDITIONS

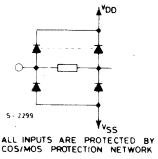
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC AND TIMING DIAGRAMS (One of three serial adders)

For 4032B

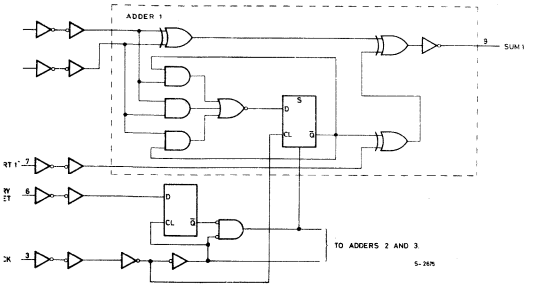


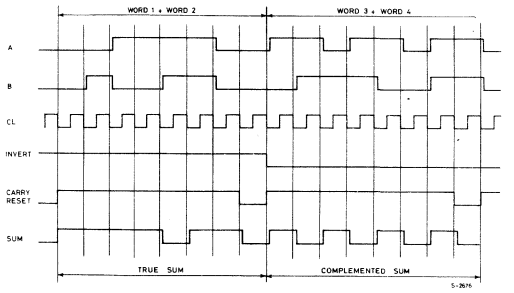


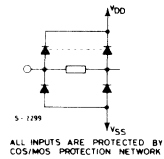


WORD 1	0.0111100 = + 60	WORD 3	1.1011011 = - 37
WORD 2	0.0110010 = + 50	WORD 4	1.1001110 = - 50
	0.1101110 = + 110		1.0101001 = - 87

For 4038B







WORD 1	1.1000011 = - 61	WORD 3	0.0100100 = + 36
WORD 2	1.1001101 = - 51	WORD 4	0.0110001 = + 49
	1.0010000 = - 112		0.1010101 = + 85

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
C_i	Input capacitance			Any input						5	7.5			pF

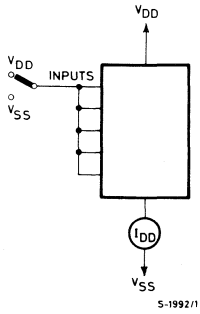
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

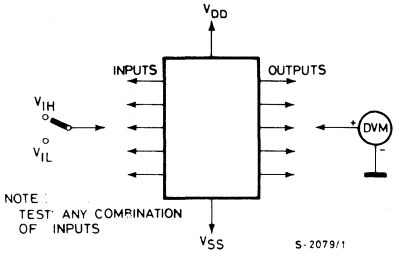
Parametric		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation delay time A, B, or Inverter Inputs to Sum Outputs	5		280		ns
		10		120		
		15		90		
t_{PHL}, t_{PLH}	Propagation delay time (Clock input to Sum Outputs)	5		500		
		10		180		
		15		135		
t_{THL}, t_{THL}	Transition time	5		100		ns
		10		50		
		15		40		
t_{hold}	Data input hold time (Clock Edge to A, B, or Reset inputs)	5		0		ns
		10		0		
		15		0		
f_{max}	Maximum clock input frequency	5		4		MHz
		10		10		
		15		12		
t_r, t_f	Clock input rise or fall time	5		15		μs
		10		15		
		15		15		

TEST CIRCUITS

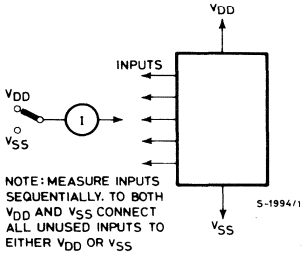
Quiescent device current



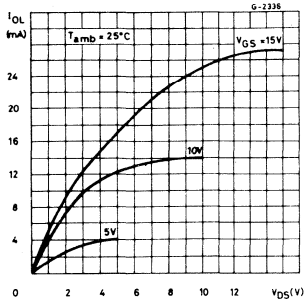
Input voltage



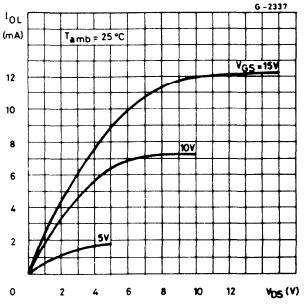
Input current



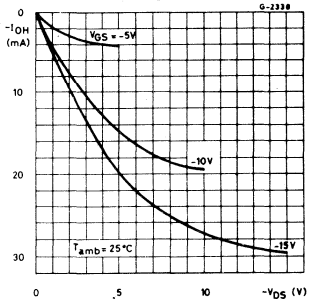
Typical output low (sink) current



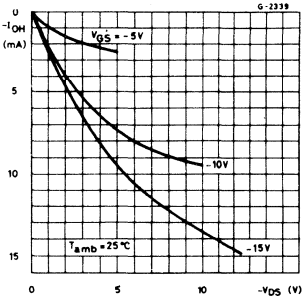
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics



Minimum output high (source) current characteristics



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

8-STAGE STATIC BIDIRECTIONAL PARALLEL/SERIAL INPUT/OUTPUT BUS REGISTER

- BIDIRECTIONAL PARALLEL DATA INPUT
- PARALLEL OR SERIAL INPUTS/PARALLEL OUTPUTS
- ASYNCHRONOUS OR SYNCHRONOUS PARALLEL DATA LOADING
- PARALLEL DATA-INPUT ENABLE ON "A" DATA LINES (3-STATE OUTPUT)
- DATA RECIRCULATION FOR REGISTER EXPANSION
- MULTIPACKAGE REGISTER EXPANSION
- FULLY STATIC OPERATIONAL DC-TO-5 MHz (TYP.) AT V_{DD}= 10V
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4034B** (extended temperature range) and **HCF 4034B** (intermediate temperature range) are monolithic integrated circuits, available in 24-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4034B** is a static eight-stage parallel-or serial-input parallel-output register. It can be used to: 1) bidirectionally transfer parallel information between two buses; 2) convert serial data to parallel form and direct the parallel data to either of two buses; 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S). Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (3-state outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided. All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

PARALLEL OPERATION – A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow. The AE-input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high. Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

SERIAL OPERATION – A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed). The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high). Register expansion can be accomplished by simply cascading **HCC/HCF 4034B** packages.

ORDERING NUMBERS:

HCC 4034 BD for dual in-line ceramic slam package
HCF 4034 BD for dual in-line ceramic slam package
HCF 4034 BE for dual in-line plastic package

HCC/HCF 4034 B

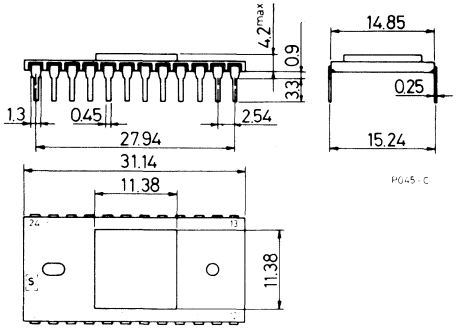
ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

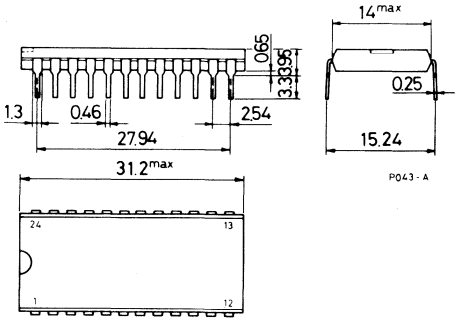
* All voltage values are referred to V_{SS} pin voltage

MECHANICAL DATA (dimensions in mm)

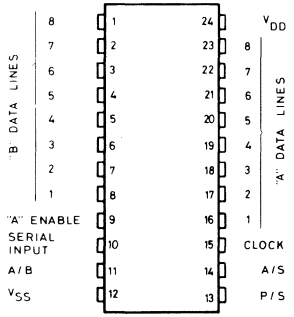
Dual in-line ceramic slam package
for **HCC/HCF 4034 BD**



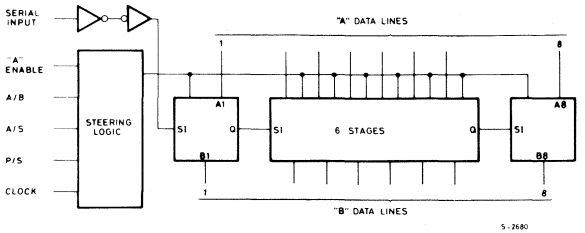
Dual in-line plastic package
for **HCF 4034 BE**



CONNECTION DIAGRAM

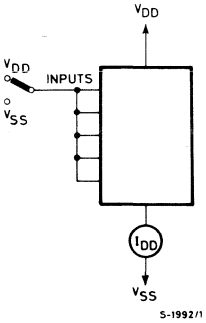


FUNCTIONAL DIAGRAM

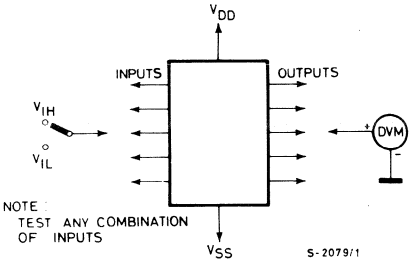


TEST CIRCUITS

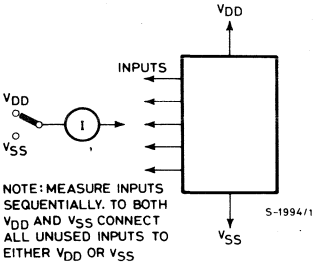
Quiescent device current



Input voltage

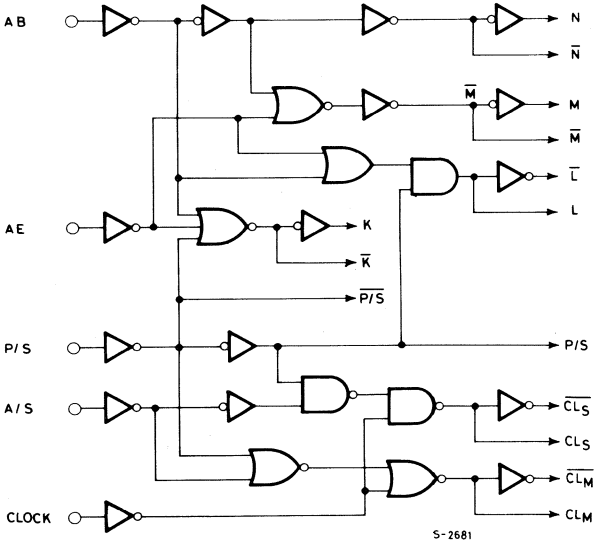


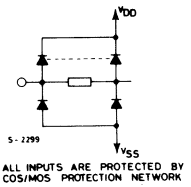
Input current



LOGIC DIAGRAM

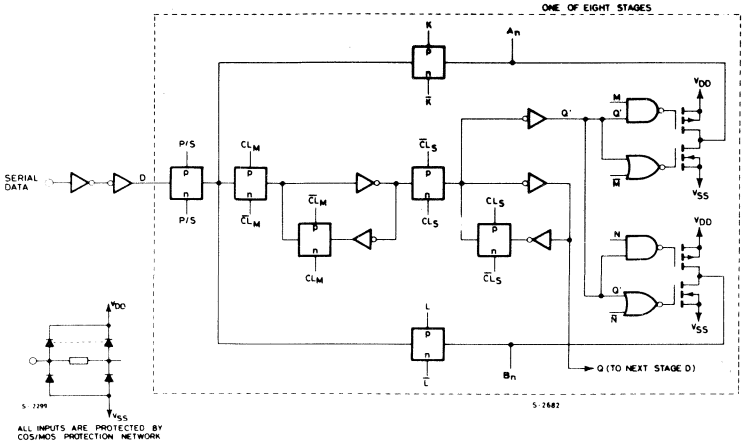
Steering logic





LOGIC DIAGRAM AND TRUTH TABLE

Register stage (1 of 8 stages)



INPUTS			OUT
$\overline{CL}_M$▲	$\overline{CL}_S$▲	D	Q
↓	↓	0	0
↑	↑	0	0
↓	↑	0	•
↑	↓	X	0
↓	↓	1	1
↑	↑	1	1
↓	↑	1	•

▲ = LEVEL CHANGE
• = INVALID CONDITION

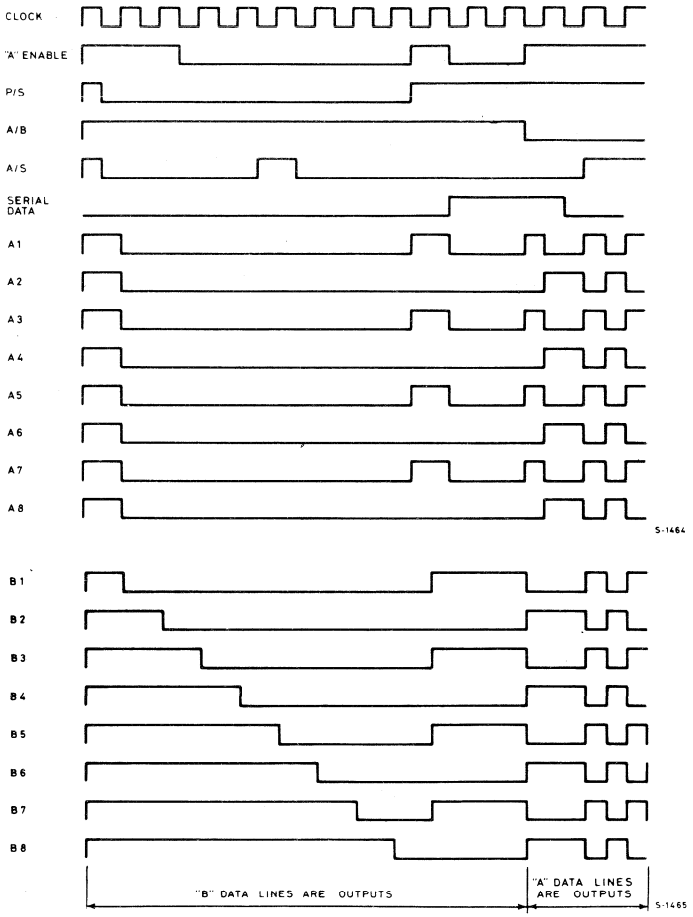
For register input-levels and resulting register operation

"A" Enable	P/S	A/B	A/S	Operation*
0	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
0	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
0	1	0	0	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
0	1	1	0	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation
0	1	1	1	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation
1	0	0	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
1	0	1	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
1	1	0	0	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
1	1	0	1	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
1	1	1	0	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
1	1	1	1	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

* Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode.

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE

TIMING DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
	Output leakage current •		0/18			18		±0.4		±10^{-4}	±0.4		± 12	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

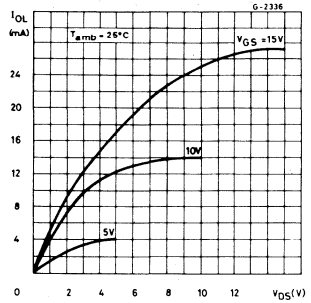
** All inputs except A and B Lines.

• A or B Lines when they are Inputs.

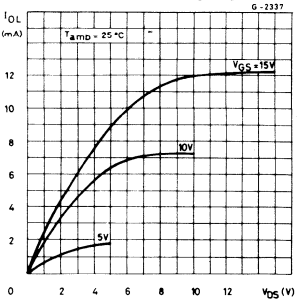
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Paramater		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time	5		750		ns
		10		300		
		15		140		
t_{THL}, t_{TLH}	Transition time	5		100		ns
		10		50		
		15		40		
f_{CL}	Maximum clock input frequency	5		2.5		MHz
		10		5		
		15		6		
t_{WC}	Clock pulse width	5		200		ns
		10		100		
		15		80		
t_W	High-Level pulse width AE, P/S, A/S	5		240		ns
		10		85		
		15		40		
t_r, t_f	Clock input rise or fall time	5		15		μs
		10		15		
		15		15		
t_{setup}	Data setup time	5		250		ns
		10		100		
		15		70		

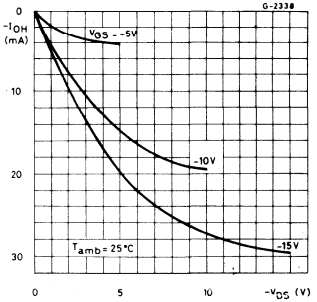
Typical output low (sink) current characteristics



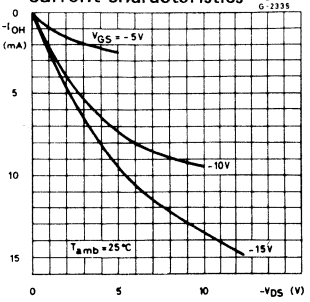
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics

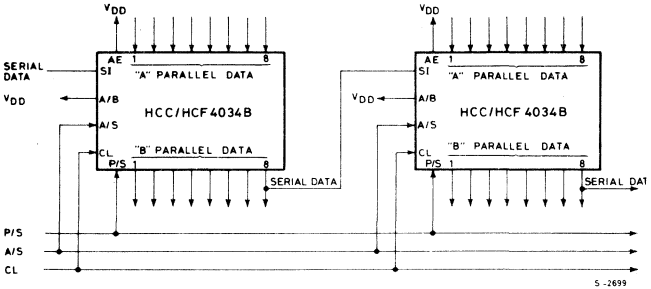


Minimum output high (source) current characteristics

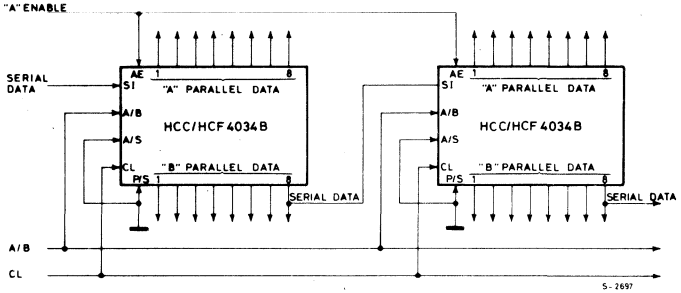


TYPICAL APPLICATIONS

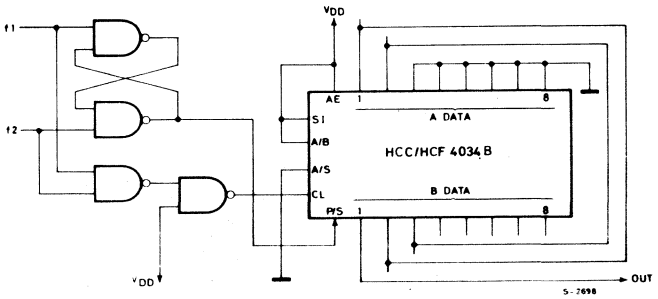
16-bit parallel in/parallel out, parallel in/serial out, serial in/parallel out, serial in/serial out register.



16-bit serial in/gated parallel out register

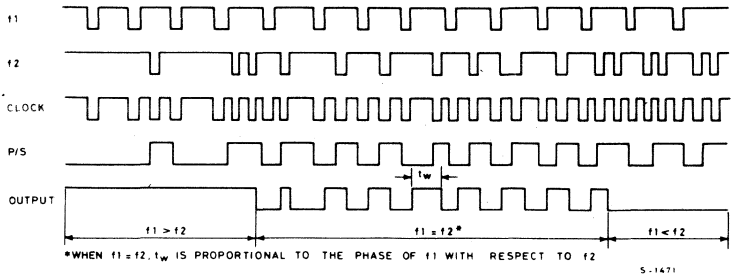


Frequency and phase comparator

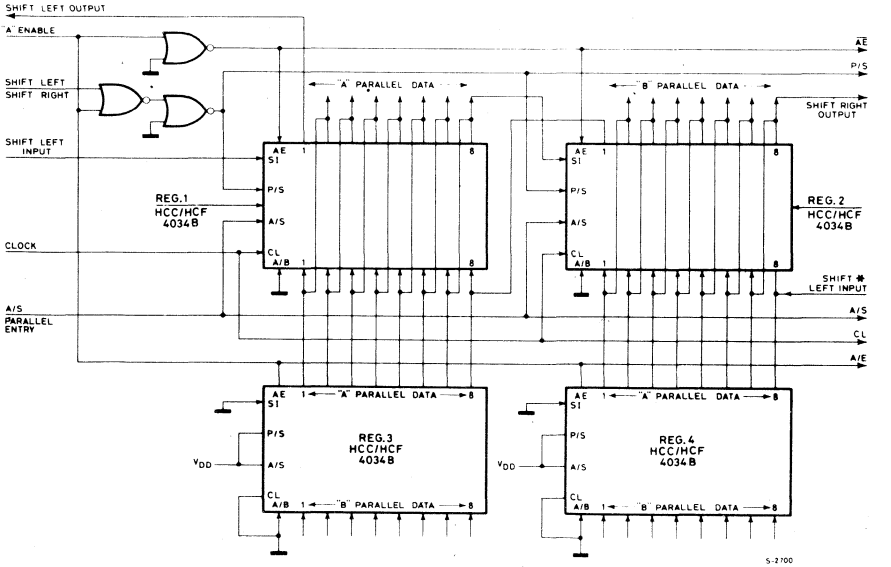


TYPICAL APPLICATIONS (continued)

Timing diagram



Shift right/shift left with parallel inputs

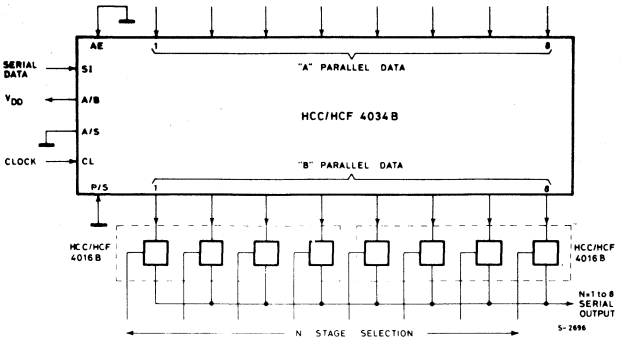


A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading. When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

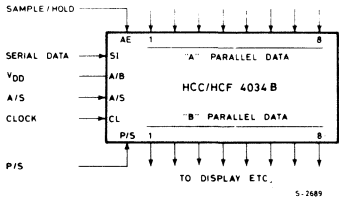
* Shift Left input must be disabled during parallel entry.

TYPICAL APPLICATIONS (continued)

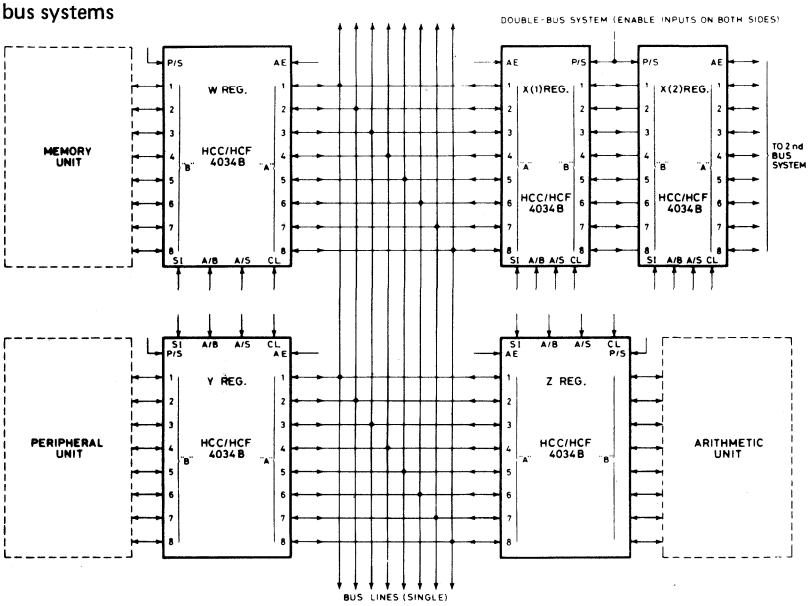
N-stage register with fixed serial output line



Sample and hold register-serial/parallel in-parallel out.



Single - and double - bus systems



The "A" enable (AE) and A/B signals control all combinations of transfer between the registers and bus systems.

COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

4-STAGE PARALLEL IN/PARALLEL OUT SHIFT REGISTER

- 4-STAGE CLOCKED SHIFT OPERATION
- SYNCHRONOUS PARALLEL ENTRY ON ALL 4 STAGES
- $J\overline{K}$ INPUTS ON FIRST STAGE
- ASYNCHRONOUS TRUE/COMPLEMENT CONTROL ON ALL OUTPUTS
- STATIC FLIP-FLOP OPERATION; MASTER-SLAVE CONFIGURATION
- BUFFERED INPUTS AND OUTPUTS
- HIGH SPEED 12 MHz (TYP.) AT V_{DD}= 10V
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4035B** (extended temperature range) and **HCF 4035B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4035B** is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via $J\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low). Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high. In the parallel or serial mode information is transferred on positive clock transitions. When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal. $J\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With $J\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

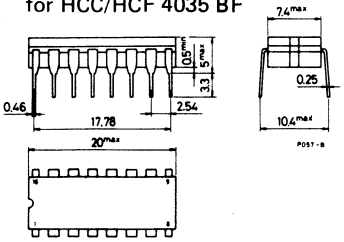
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

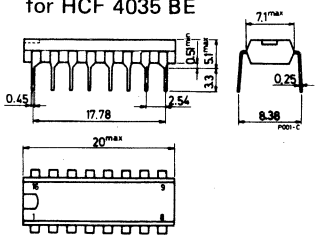
HCC 4035 BD for dual in-line ceramic package
HCC 4035 BF for dual in-line ceramic package, frit seal
HCC 4035 BK for ceramic flat package
HCF 4035 BE for dual in-line plastic package
HCF 4035 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

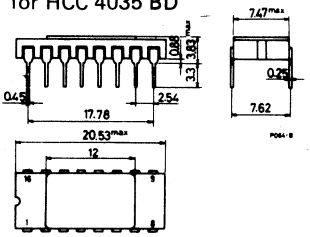
Dual in-line ceramic package
for HCC/HCF 4035 BF



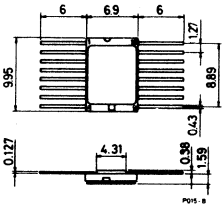
Daul in-line plastic package
for HCF 4035 BE



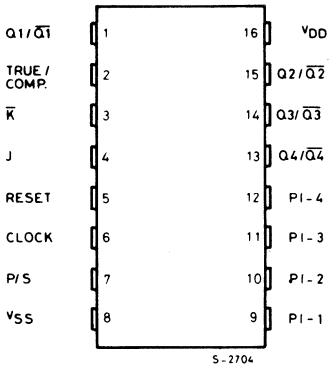
Dual in-line ceramic package
for HCC 4035 BD



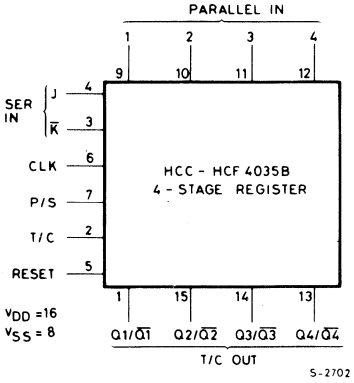
Ceramic flat package
for HCC 4035 BK



CONNECTION DIAGRAM



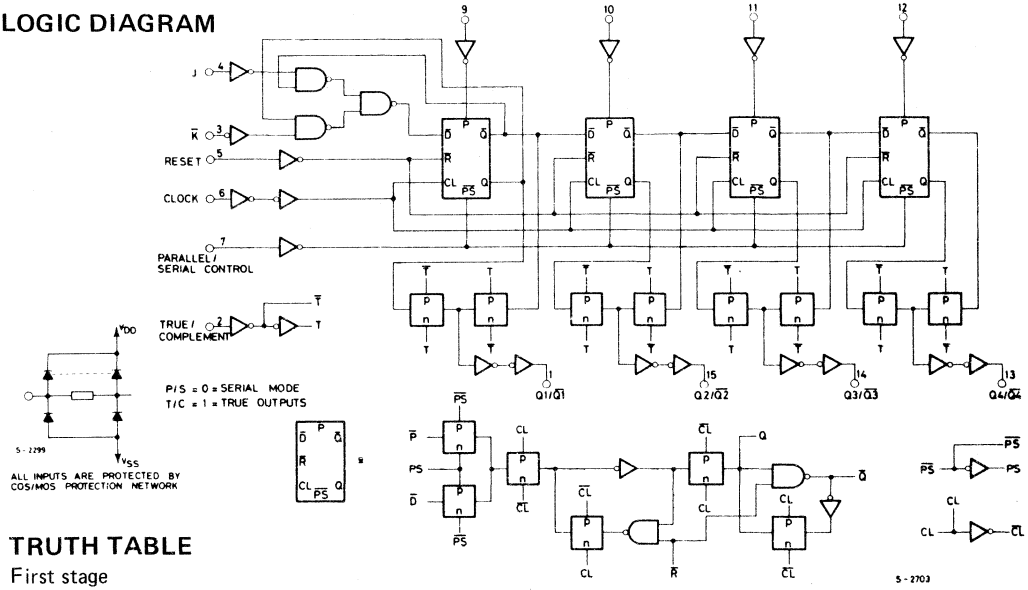
FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM



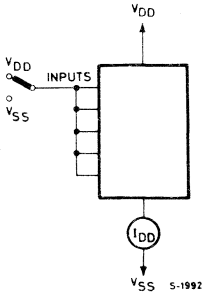
TRUTH TABLE

First stage

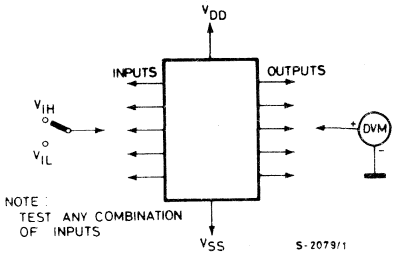
CLOCK (ϕ)	t_{n-1} (INPUTS)				t_n (OUTPUTS)
	J	$\bar{K}$	R	Q_{n-1}	Q_n
⌐¯	0	X	0	0	0
⌐¯	1	X	0	0	1
⌐¯	X	0	0	1	0
⌐¯	1	0	0	Q_{n-1}	$\bar{Q}_{n-1}$ TOGGLE MODE
⌐¯	X	1	0	1	1
¯⌐	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

TEST CIRCUITS

Quiescent device current

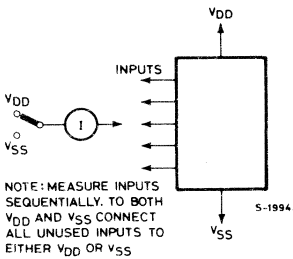


Input voltage



NOTE: TEST ANY COMBINATION OF INPUTS

Input current



NOTE: MEASURE INPUTS SEQUENTIALLY. TO BOTH V_{DD} AND V_{SS} CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		$\pm$0.1		$\pm 10^{-5}$	$\pm$0.1		$\pm$ 1	μA
C_I**	Input capacitance									5	7.5			pF

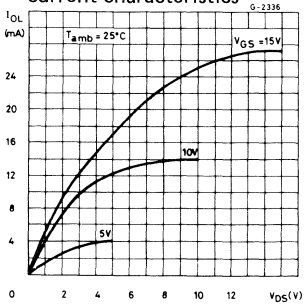
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

** Any input

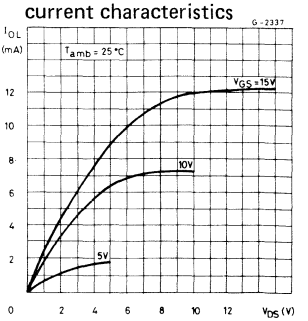
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
	V_{DD} (V)	Min.	Typ.	Max.	
CLOCKED OPERATION					
t_{PLH}, t_{PHL} Propagation delay time	5		200		ns
	10		100		
	15		80		
t_{THL}, t_{TLH} Transition time	5		100		ns
	10		50		
	15		40		
f_{CL} Maximum clock input frequency	5		5		MHz
	10		12		
	15		16		
t_{WC} Clock pulse width	5		100		ns
	10		45		
	15		30		
t_r, t_f Clock input rise or fall time	5		15		μs
	10		15		
	15		15		
t_{setup} Data setup time J/$\overline{K}$ Lines	5		50		ns
	10		25		
	15		20		
t_{setup} Data setup time Parallel – In – Lines	5		25		ns
	10		15		
	15		10		
RESET OPERATION					
t_{PLH}, t_{PHL} Propagation delay time	5		200		ns
	10		100		
	15		80		
t_{WR} Reset pulse width	5		100		ns
	10		45		
	15		30		

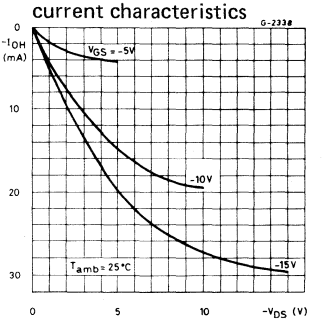
Typical output low (sink) current characteristics



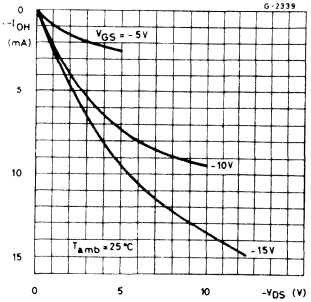
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics

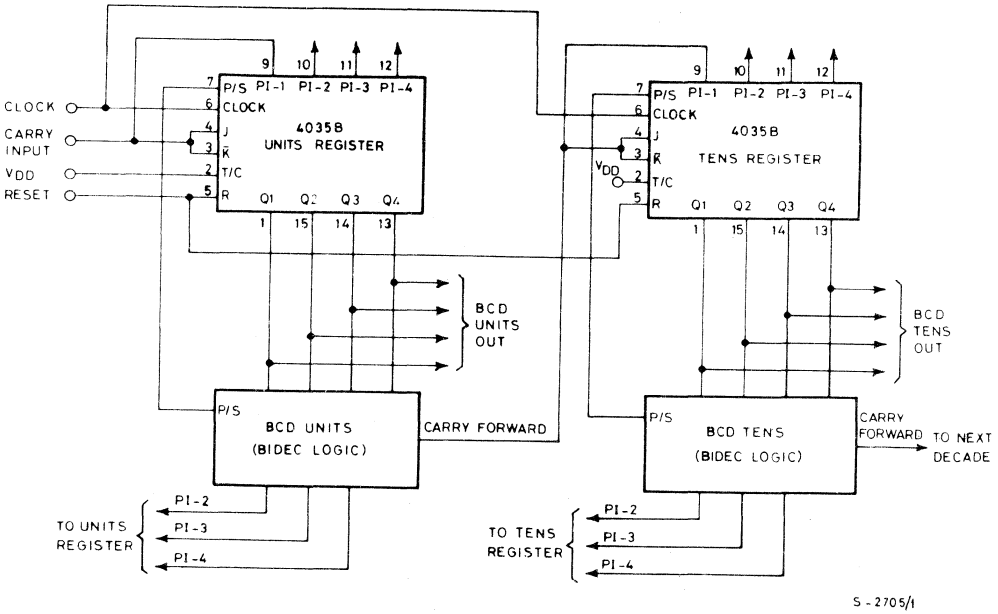


Minimum output high (source) current characteristics



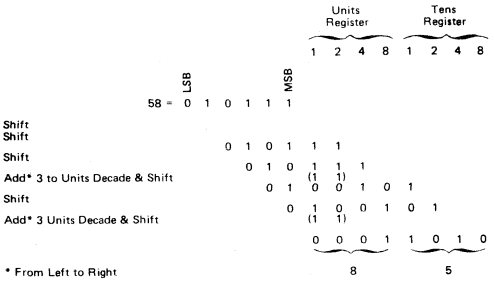
TYPICAL APPLICATIONS

Binary - to - BCD converter

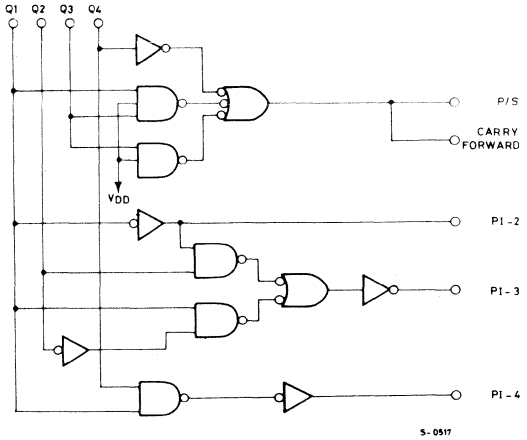


TYPICAL APPLICATIONS (continued)

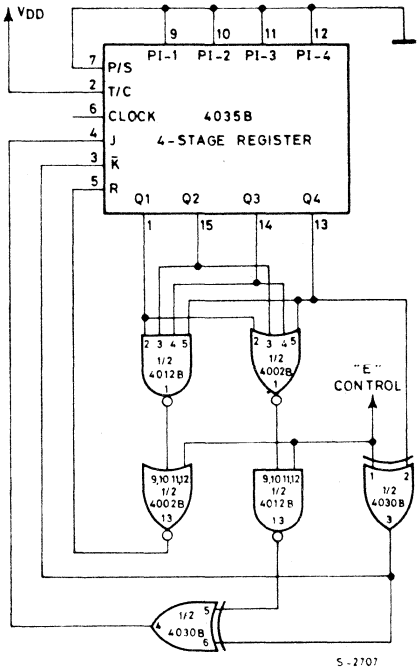
Example of binary-to-BCD conversion



BIDEC logic



Double sequence generator

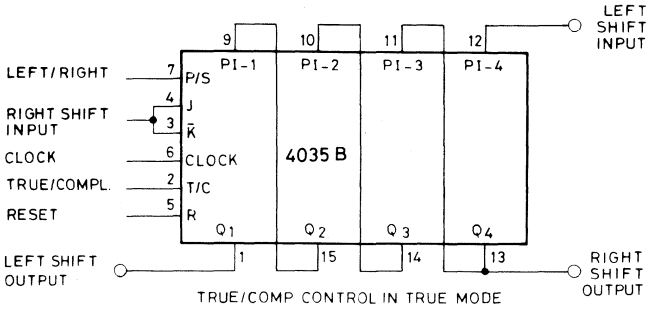


State sequences

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E).

Control = E = 0						1				
	Q_1 A	Q_2 B	Q_3 C	Q_4 D			Q_1 A	Q_2 B	Q_3 C	Q_4 D
0	0	0	0	0		15	1	1	1	1
1	1	0	0	0		14	0	0	1	1
2	0	1	0	0		13	1	0	1	1
5	1	0	1	0		10	0	1	0	1
10	0	1	0	1		5	1	0	1	0
4	0	0	1	0		11	1	1	0	1
9	1	0	0	1		6	0	1	1	0
3	1	1	0	0		12	0	0	1	1
6	0	1	1	0		9	1	0	0	1
13	1	0	1	1		2	0	1	0	0
11	1	1	0	1		4	0	0	1	0
7	1	1	1	0		8	0	0	0	1
14	0	1	1	1		1	1	0	0	0
12	0	0	1	1		3	1	1	0	0
8	0	0	0	1		7	1	1	1	0

Shift left/shift right register



COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4041 UB

PRELIMINARY DATA

QUAD TRUE/COMPLEMENT BUFFER

- BALANCED SINK AND SOURCE CURRENT; APPROXIMATELY 4 TIMES STANDARD "B" DRIVE
- EQUALIZED DELAY TO TRUE AND COMPLEMENT OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT LEAKAGE CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V AND 15V PARAMETRIC RATINGS

The **HCC 4041 UB** (extended temperature range) and **HCF 4041 UB** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4041 UB** types are quad true/complement buffers consisting of n- and p-channel units having low channel resistance and high current (sourcing and sinking) capability. The **HCC/HCF 4041 UB** is intended for use as a buffer, line driver, or COS/MOS-to-TTL driver. It can be used as an ultra-low power resistor-network driver for A/D and D/A conversion, as a transmission-line driver, and in other applications where high noise immunity and low-power dissipation are primary design requirements.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

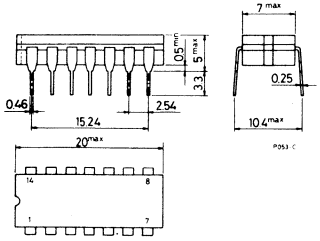
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

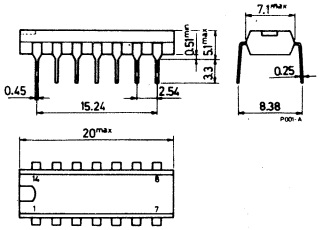
HCC 4041 UBD for dual in-line ceramic package
HCC 4041 UBF for dual in-line ceramic package, frit seal
HCC 4041 UBK for ceramic flat package
HCF 4041 UBE for dual in-line plastic package
HCF 4041 UBF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

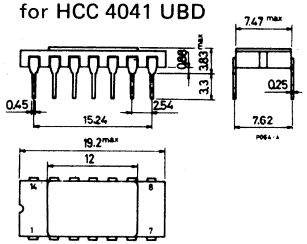
Dual in-line ceramic package
for HCC/HCF 4041 UBF



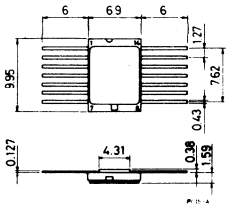
Dual in-line plastic package
for HCF 4041 UBE



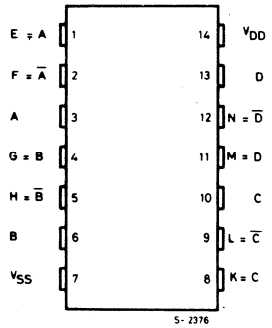
Dual in-line ceramic package
for HCC 4041 UBD



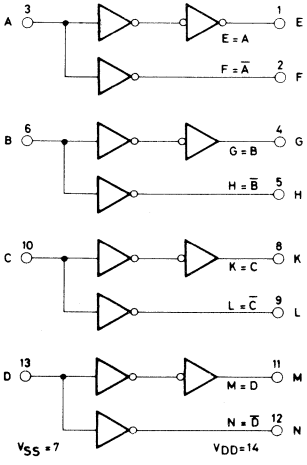
Ceramic flat package
for HCC 4041 UBK



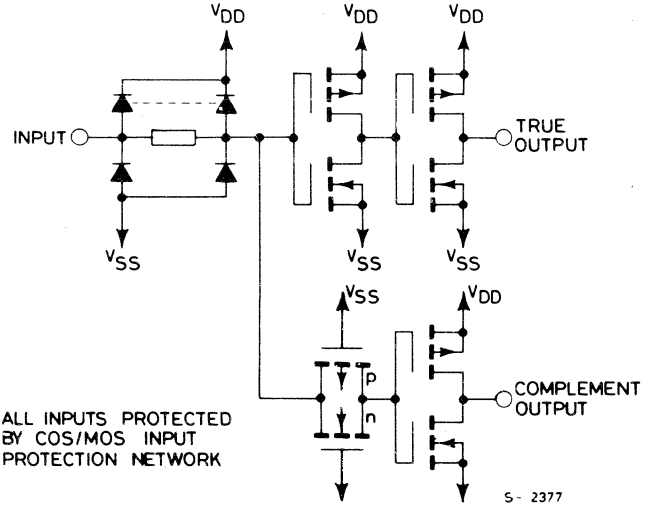
CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

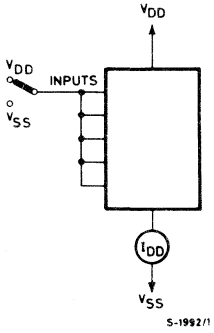


SCHEMATIC DIAGRAM

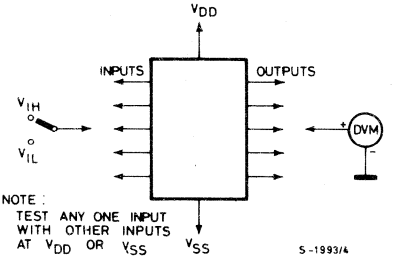


TEST CIRCUITS

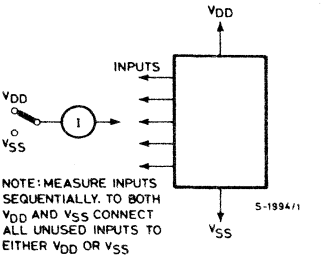
Quiescent device current



Noise immunity



Input leakage current



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (under recommended operating conditions)

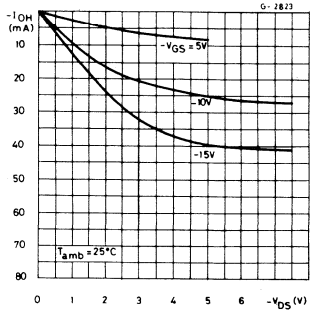
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	4		4			4		V
				1/9	< 1	10	8		8			8		
				1.5/13.5	< 1	15	12		12			12		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1			1		1	V
				9/1	< 1	10		2			2		2	
				13.5/1.5	< 1	15		3			3		3	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-8.4		-6.4	-12.8		-4.6		mA
			0/ 5	4.6		5	-2.1		-1.6	-3.2		-1.2		
			0/10	9.5		10	-6.25		-5	-10		-3.5		
			0/15	13.5		15	-24		-19	-38		-13		
		HCF types	0/ 5	2.5		5	-6.7		-6.4	-12.8		-5.4		
			0/ 5	4.6		5	-1.8		-1.6	-3.2		-1.44		
			0/10	9.5		10	-5.6		-5	-10		-4.5		
			0/15	13.5		15	-23		-19	-38		-17		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	2.1		1.6	3.2		1.2		mA
			0/10	0.5		10	6.25		5	10		3.5		
			0/15	1.5		15	24		19	38		13		
		HCF types	0/ 5	0.4		5	1.8		1.6	3.2		1.44		
			0/10	0.5		10	5.6		5	10		4.5		
			0/15	1.5		15	23		19	38		17		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		± 0.1		± 10^{-5}	± 0.1		± 1	μA
C_I**	Input capacitance									15	22.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
** Any input

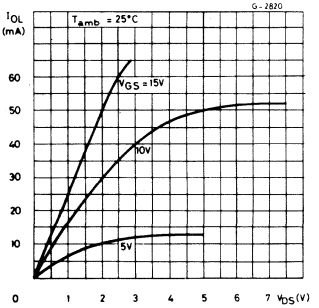
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
	V_{DD}(V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time	5		60	120	ns
	10		35	70	
	15		25	50	
t_{THL}, t_{TLH} Transition time	5		40	80	ns
	10		20	40	
	15		15	30	

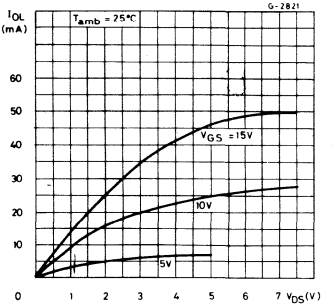
Minimum output high (source) current characteristics



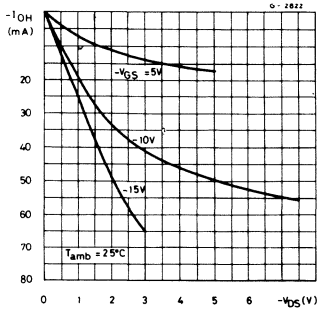
Typical output low (sink) current



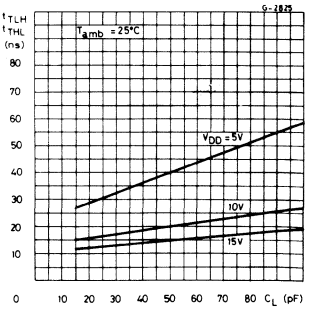
Minimum output low (sink) current characteristics



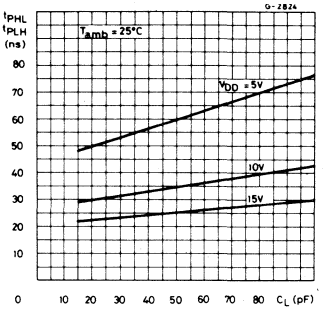
Typical output high (source) current characteristics



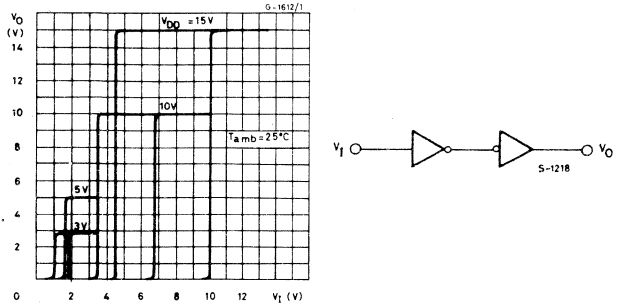
Typical transition time vs. load capacitance



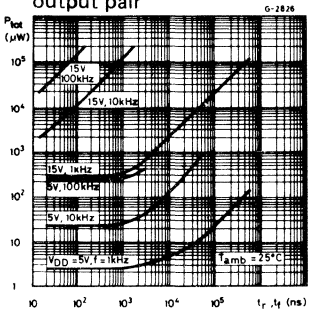
Typical propagation delay time vs. load capacitance



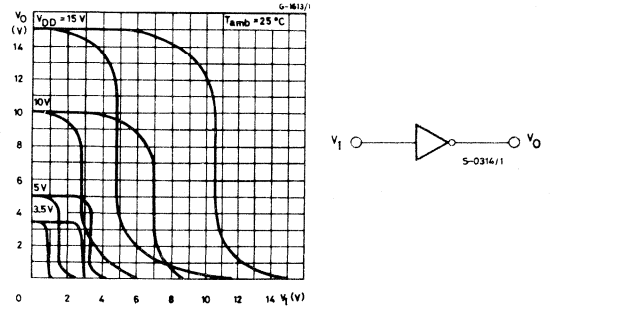
Minimum and maximum transfer characteristics–true output-and test circuit



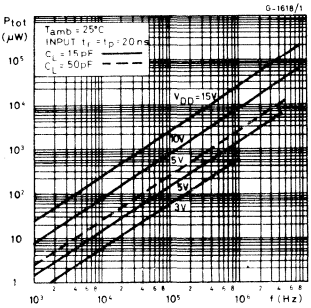
Typical power dissipation vs. input rise and fall time per output pair



Minimum maximum transfer characteristics complement output-and test circuit



Typical power dissipation vs. frequency per output pair



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

QUAD CLOCKED "D" LATCH

- CLOCK POLARITY CONTROL
- Q AND $\overline{Q}$ OUTPUTS
- COMMON CLOCK
- LOW POWER TTL COMPATIBLE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V AND 15V PARAMETRIC RATINGS

The **HCC 4042B** (extended temperature range) and **HCF 4042B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4042B** types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical.
Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

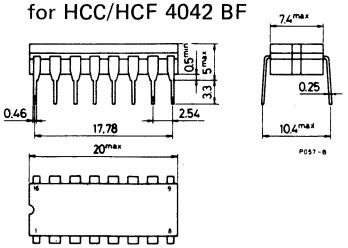
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

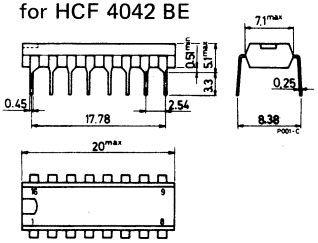
HCC 4042 BD for dual in-line ceramic package
HCC 4042 BF for dual in-line ceramic package, frit seal
HCC 4042 BK for ceramic flat package
HCF 4042 BE for dual in-line plastic package
HCF 4042 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

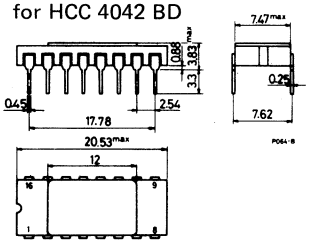
Dual in-line ceramic package for HCC/HCF 4042 BF



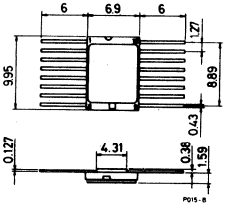
Dual in-line plastic package for HCF 4042 BE



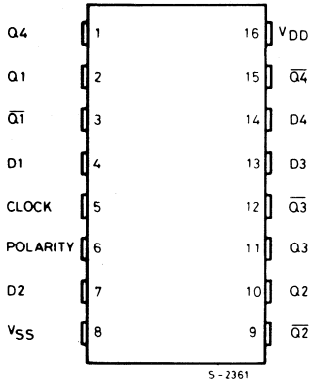
Dual in-line ceramic package for HCC 4042 BD



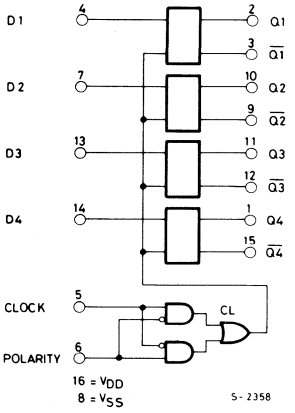
Ceramic flat package for HCC 4042 BK



CONNECTION DIAGRAM



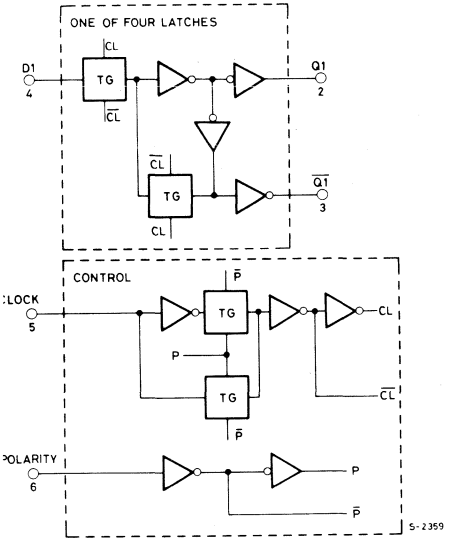
FUNCTIONAL DIAGRAM



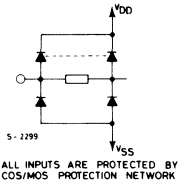
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC BLOCK DIAGRAM AND TRUTH TABLE

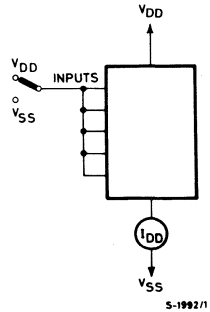


CLOCK	POLARITY	Q
0	0	D
↗	0	LATCH
1	1	D
↘	1	LATCH

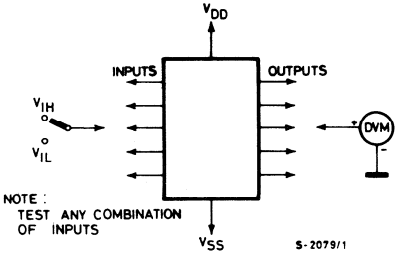


TEST CIRCUITS

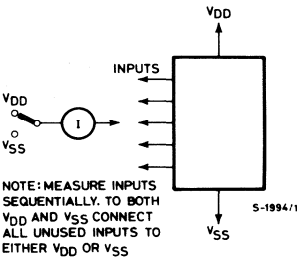
Quiescent device current



Noise immunity



Input leakage current



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

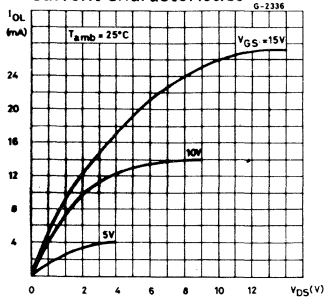
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		± 0.1		± 10^{-5}	± 0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

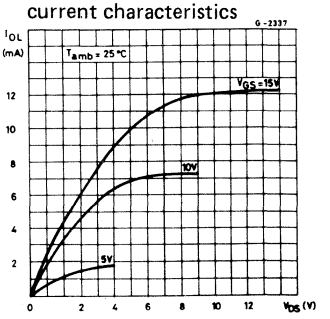
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter			Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time	Data In to Q	5		110	220	ns
			10		55	110	
			15		40	80	
		Data In to $\overline{Q}$	5		150	300	
			10		75	150	
			15		50	100	
		Clock to Q	5		225	450	
			10		100	200	
			15		80	160	
		Clock to $\overline{Q}$	5		250	500	
			10		115	230	
			15		90	180	
t_{THL}, t_{TLH}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Clock pulse width		5	200	100		ns
			10	100	50		
			15	60	30		
t_{setup}	Setup time		5	50	0		ns
			10	30	0		
			15	25	0		
t_{hold}	Hold time		5	120	60		ns
			10	60	30		
			15	50	25		
t_r, t_f	Clock input rise or fall time		5	Not rise or fall time sensitive			μs
			10				
			15				

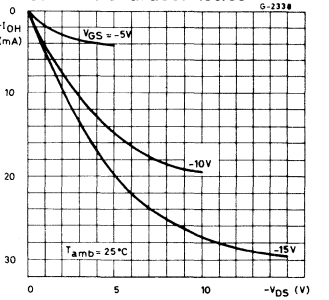
Typical output low (sink) current characteristics



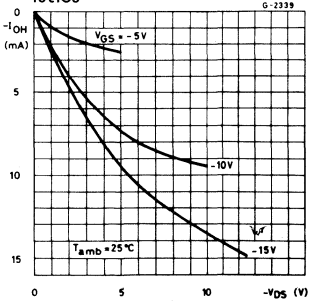
Minimum output low (sink) current characteristics



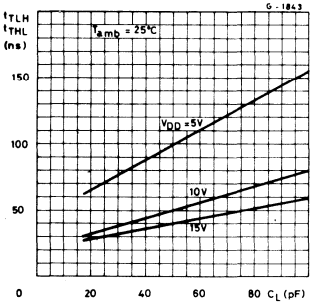
Typical output high (source) current characteristics



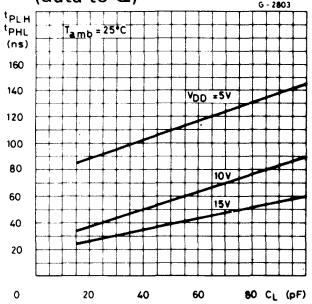
Minimum output high (source) current characteristics



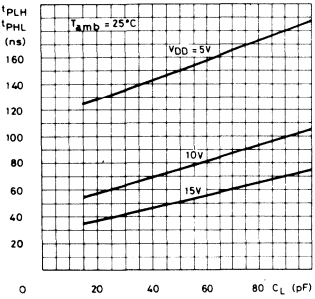
Typical transition time vs. load capacitance



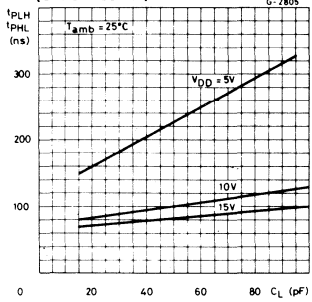
Typical propagation delay time vs. load capacitance (data to Q)



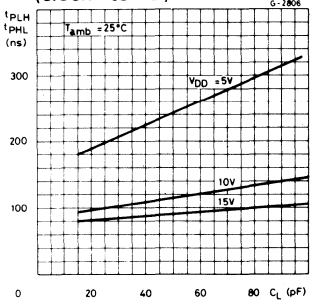
Typical propagation delay time vs. load capacitance (data to $\overline{Q}$)



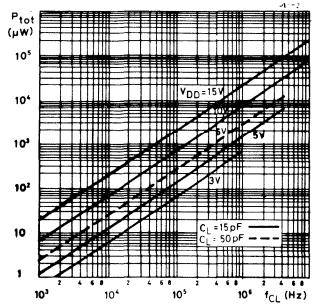
Typical propagation delay time vs. load capacitance (clock to Q)



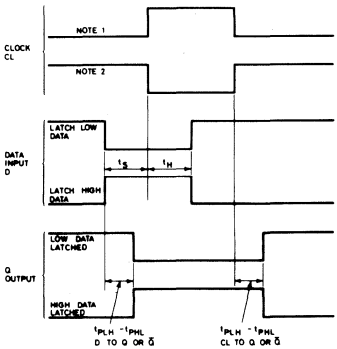
Typical propagation delay time vs. load capacitance (clock to $\overline{Q}$)



Typical power dissipation/ device vs. frequency



Dynamic test parameters



NOTES:
1. FOR POSITIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS LOW.
2. FOR NEGATIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS HIGH.

HCC/HCF 4043B
HCC/HCF 4044B

PRELIMINARY DATA

QUAD 3-STATE R-S LATCHES: QUAD NOR R-S LATCH-4043B
QUAD NAND R-S LATCH-4044B

- QUIESCENT CURRENT SPECIFIED TO 20V
- MAX. INPUT LEAKAGE CURRENT 1 μA @ 18V (FULL PACKAGE TEMP. RANGE)
- 3-LEVEL OUTPUTS WITH COMMON OUTPUT ENABLE
- SEPARATE SET and RESET INPUT for EACH LATCH
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- NOR and NAND CONFIGURATIONS

The **HCC 4043B, HCC 4044B**, (extended temperature range) and the **HCF 4043B, HCF 4044B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4043B** types are quad cross-coupled 3-state COS/MOS NOR latches and the **HCC/HCF 4044B** types are quad cross-coupled 3-state COS/MOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or "high" on the ENABLE input connects the latch states to the Q outputs. A logic "0" or "low" on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common bussing of the outputs.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

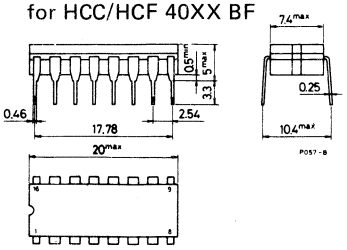
ORDERING NUMBERS:

HCC 40XX BD for dual in-line ceramic package
HCC 40XX BF for dual in-line ceramic package, frit seal
HCC 40XX BK for ceramic flat package
HCF 40XX BE for dual in-line plastic package
HCF 40XX BF for dual in-line ceramic package, frit seal

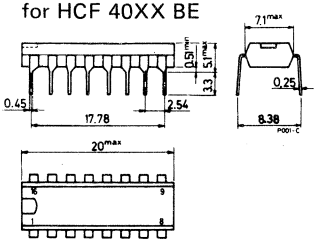
HCC/HCF 4043B
HCC/HCF 4044B

MECHANICAL DATA (dimensions in mm)

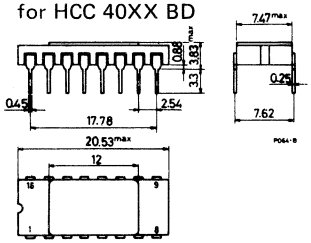
Dual in-line ceramic package for HCC/HCF 40XX BF



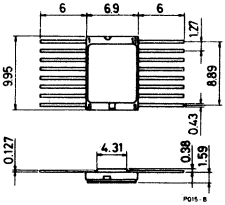
Dual in-line plastic package for HCF 40XX BE



Dual in-line ceramic package for HCC 40XX BD

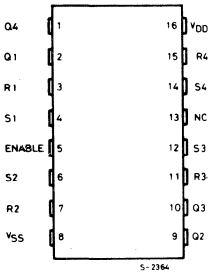


Ceramic flat package for HCC 40XX BK

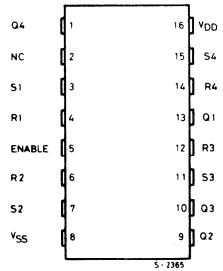


CONNECTION DIAGRAMS

For **4043B**

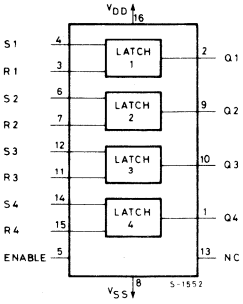


For **4044B**

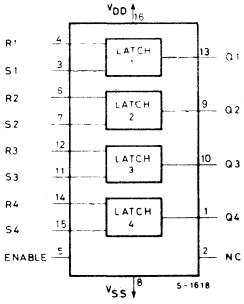


FUNCTIONAL DIAGRAMS

For **4043B**



For **4044B**

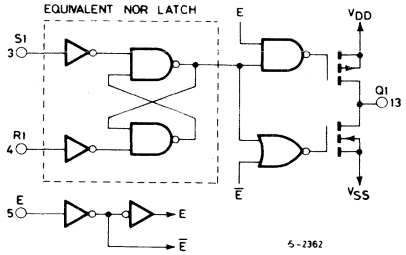


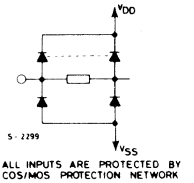
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

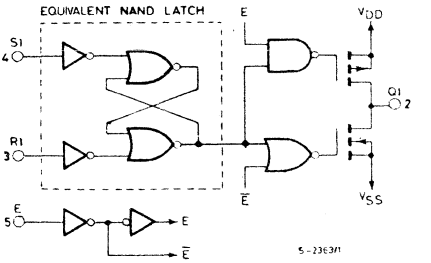
LOGIC DIAGRAMS

For **4043B**



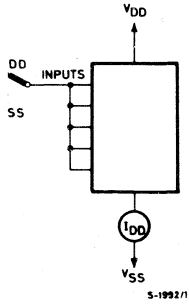


For **4044B**

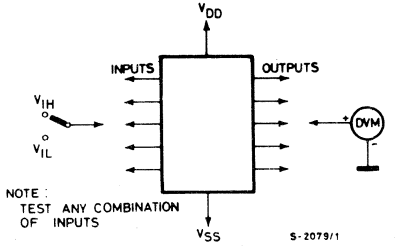


TEST CIRCUITS

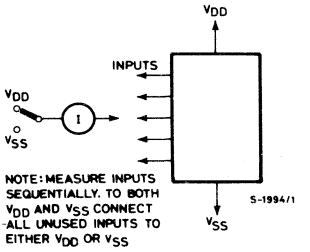
Quiescent device current



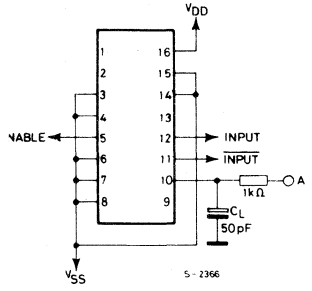
Input voltage



Input current

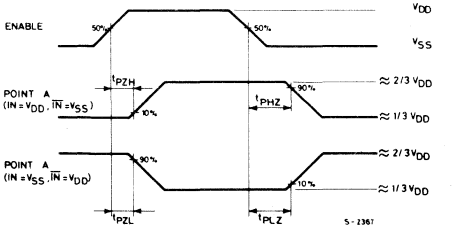


ENABLE propagation delay time and waveforms



TEST	IN	$\overline{IN}$	A
t_{PHZ}	V_{DD}	V_{SS}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}	V_{SS}
t_{PZL}	V_{SS}	V_{DD}	V_{DD}

Z = HIGH IMPEDANCE



STATIC ELECTRICAL CHARACTERISTICS (under recommended operating conditions)

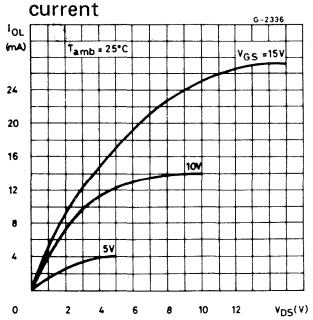
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				2/13	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13/2	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
I_{OH}	3-state output		0/18	0/18		18		± 0.4		±10^{-4}	± 0.4		± 12	μA
C_i**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

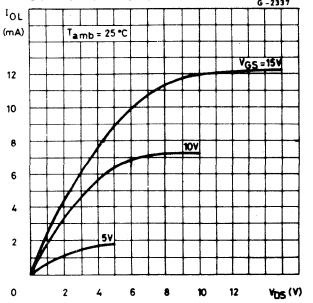
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time (SET or RESET to Q)	5		150	300	ns
		10		70	140	
		15		50	100	
t_{PZH}, t_{PHZ}	3-State propagation delay time (ENABLE to Q)	5		115	230	ns
		10		55	110	
		15		40	80	
t_{PLZ} t_{PZL}	Propagation delay time	5		90	180	ns
		10		50	100	
		15		35	70	
t_{TLH}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_W	Pulse width (SET or RESET)	5	160	80		ns
		10	80	40		
		15	40	20		

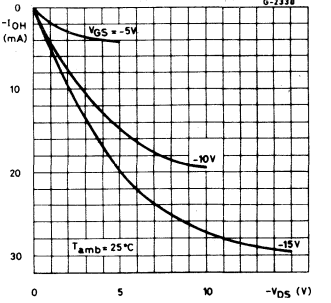
Typical output low (sink) current



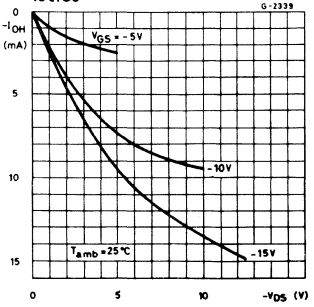
Minimum output low (sink) current characteristics



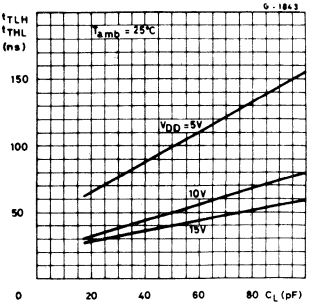
Typical output high (source) current characteristics



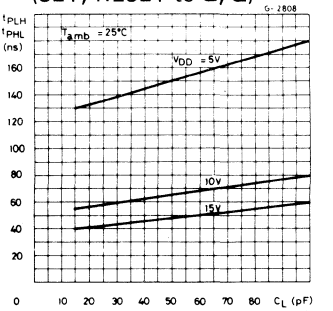
Minimum output high (source) current characteristics



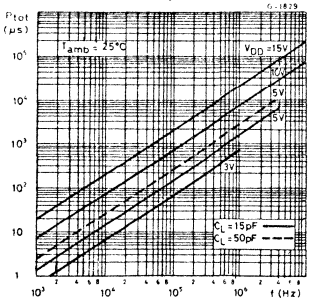
Typical transition time vs. load capacitance



Typical propagation delay time vs. load capacitance (SET, RESET to Q, $\overline{Q}$)

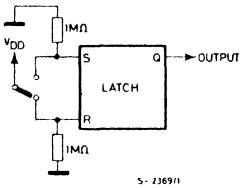


Typical power dissipation/ device vs. frequency

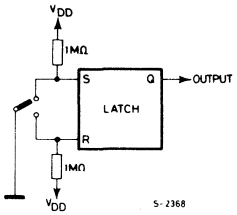


Switch bounce eliminator

for **4043B**

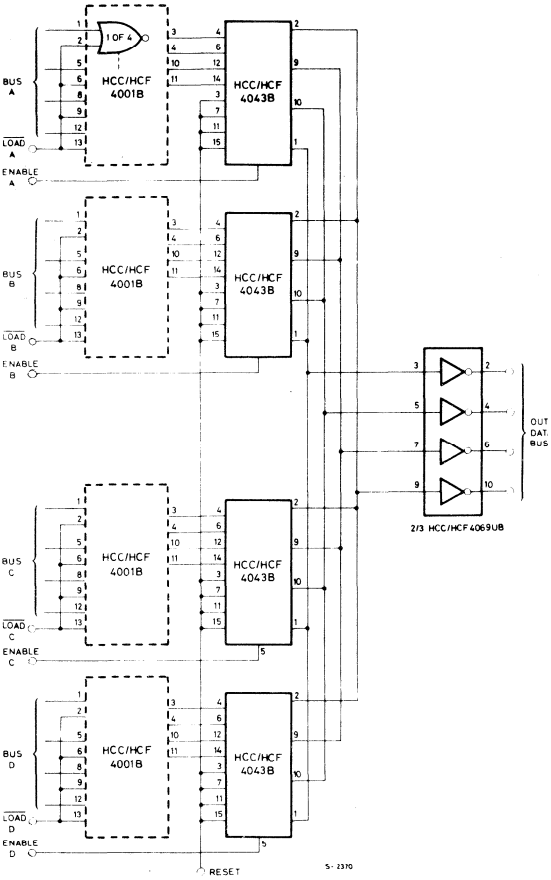


for **4044B**



APPLICATIONS

Multiple bus storage



COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4045B

PRELIMINARY DATA

COS/MOS 21-STAGE COUNTER

- VERY LOW OPERATING DISSIPATION . . . . 1 mW (TYP.); @ V_{DD}= 5V, f_ϕ = 1 MHz
- OUTPUT DRIVERS WITH SINCK OR SOURCE CAPABILITY . . . . 7 mA (TYP.) @ V_{DD}= 5V
- MEDIUM SPEED (TYP.) . . . . f_ϕ = 16 MHz, @ V_{DD}= 10V
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4045B** (extended temperature range) and **HCF 4045B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4045B** is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, and input inverters for use in a crystal oscillator. The **HCC/HCF 4045B** configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers. The first inverter is intended for use as a crystal oscillator-amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_p to V_{DD}, S_n to V_{SS}).

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

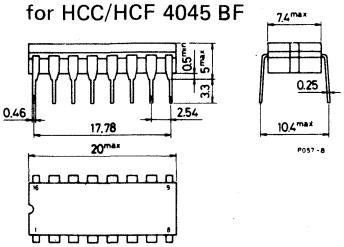
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

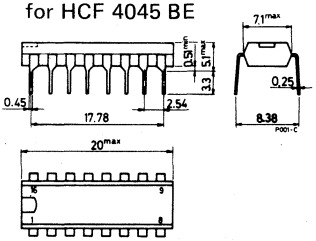
HCC 4045 BD for dual in-line ceramic package
HCC 4045 BF for dual in-line ceramic package, frit seal
HCC 4045 BK for ceramic flat package
HCF 4045 BE for dual in-line plastic package
HCF 4045 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

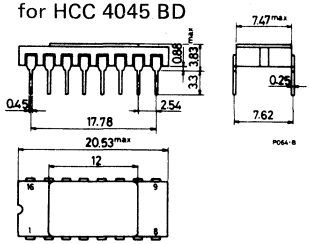
Dual in-line ceramic package
for HCC/HCF 4045 BF



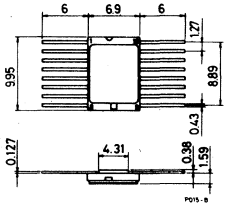
Dual in-line plastic package
for HCF 4045 BE



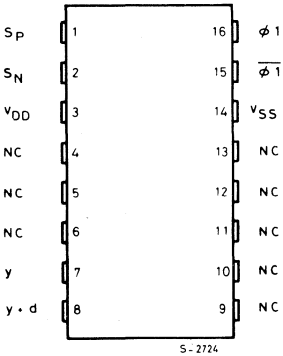
Dual in-line ceramic package
for HCC 4045 BD



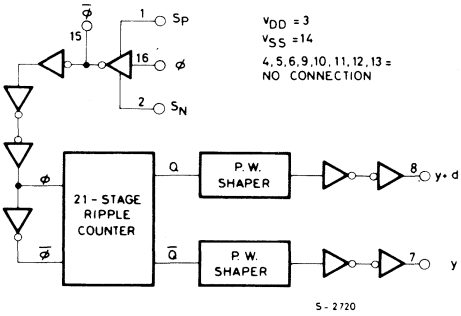
Ceramic flat package
for HCC 4045 BK



CONNECTION DIAGRAM



LOGIC DIAGRAM

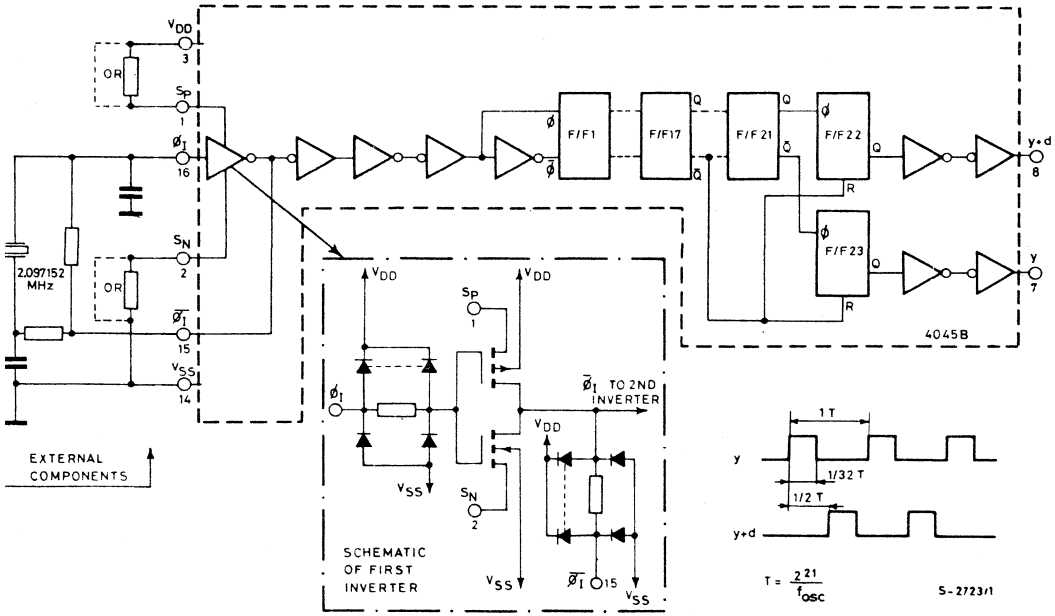


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

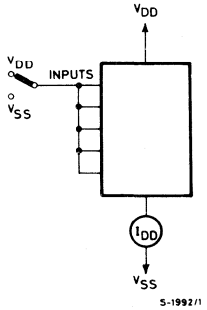
LOGIC DIAGRAM

4045B and outboard components in a typical 21-stage counter application

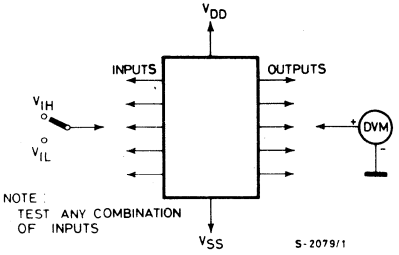


TEST CIRCUITS

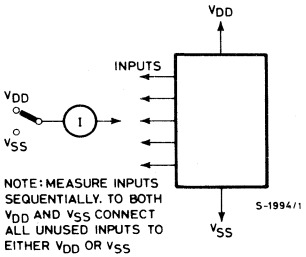
Quiescent device current



Noise immunity



Input leakage current



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions				Values							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
						Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current	0/ 5			5		5		0.04	5		150	μA
		0/10			10		10		0.04	10		300	
		0/15			15		20		0.04	20		600	
		0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage	0/ 5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage	5/0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V
			1/9	< 1	10	7		7			7		
			1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V
			9/1	< 1	10		3			3		3	
			13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	0/ 5	4.6						- 7				mA
		0/10	9.5						-18				
		0/15	13.5						-47				
I_{OL}	Output sink current	0/ 5	0.4						7				
		0/10	0.5						18				
		0/15	1.5						47				
I_{IH},I_{IL}**	Input leakage current	0/18			18		± 0.1		± 10^{-5}	± 0.1		± 1	μA
C_I**	Input capacitance								5	7.5			pF

* T_{Low}= - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High}= +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V
** Any input

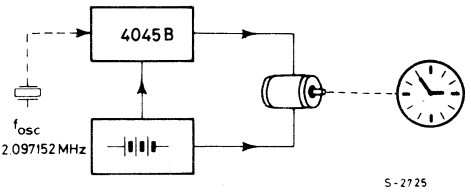
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time ϕ to y or y + d out		5		2.2		μs
			10		1.2		
			15		1		
t_{THL}, t_{TLH}	Transition time		5		100		ns
			10		50		
			15		40		
f_{max}	Maximum input pulse frequency		5		7		MHz
			10		16		
			15		24		
t_W	Input pulse width		5		100		ns
			10		50		
			15		40		
t_r, t_f	Clock input rise or fall time		5		15		μs
			10		10		
			15		10		

TYPICAL APPLICATIONS

Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.
Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.
Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.

Electronic watch application circuit



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

MICROPOWER PHASE-LOCKED LOOP

- QUIESCENT CURRENT SPECIFIED TO 20V
- VERY LOW POWER CONSUMPTION: 100 μW (TYP.) AT VCO f_o= 10 kHz, V_{DD}= 5V
- OPERATING FREQUENCY RANGE: UP TO 1.4 MHz (TYP. AT V_{DD}= 10V
- LOW FREQUENCY DRIFT: 0.06%/°C (TYP.) AT V_{DD}= 10V
- CHOICE OF TWO PHASE COMPARATORS:1) EXCLUSIVE - OR NETWORK
  2) EDGE-CONTROLLED MEMORY NETWORK WITH PHASE-PULSE OUTPUT FOR LOCK INDICATION
- HIGH VCO LINEARITY: 1% (TYP.)
- VCO INHIBIT CONTROL FOR ON-OFF KEYING AND ULTRA-LOW STANDBY POWER CONSUMPTION
- SOURCE-FOLLOWER OUTPUT OF VCO CONTROL INPUT (DEMOD. OUTPUT)
- ZENER DIODE TO ASSIST SUPPLY REGULATION
- 5V, 10V AND 15V PARAMETRIC RATING

The **HCC 4046B** (extended temperature range) and **HCF 4046B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4046B** COS/MOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2V zener diode is provided for supply regulation if necessary.

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifiers the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full COS/MOS logic swing is available at the output of the VCO and allows direct coupling to COS/MOS frequency dividers such as the **HCC/HCF 4024B, HCC/HCF 4018B, HCC/HCF 4020B, HCC/HCF 4022B, HCC/HCF 4029B,** and **HBC/HBF 4059A**. One or more **HCC/HCF 4018B** (Presettable Divide-by-N Counter) or **HCC/HCF 4029B** (Presettable Up/Down Counter), or **HBC/HBF 4059A** (Programmable Divide-by-"N" Counter), together with the **HCC/HCF 4046B** (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within COS/MOS logic levels [logic "0" $\leqslant$ 30% (V_{DD}-V_{SS}), logic "1" $\geqslant$ 70% (V_{DD}-V_{SS})]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input. Phase. comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal-and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o). The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range (2 f_c). The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range (2 f_L). The capture range is $\leqslant$ the lock range. With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent

on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal. One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. (a) shows the typical, triangular, phase-to-output response characteristic of phase-comparator I. Typical waveforms for a COS/MOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Fig. (b). Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-stage output-circuit comprising p-and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n-and p-drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n-and p-drivers OFF (3 state) the remainder of the time. If the signal and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p-and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p-and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. (c) shows typical waveforms for a COS/MOS PLL employing phase comparator II in a locked condition.

Fig. (a) - Phase-comparator I characteristics at low-pass filter output

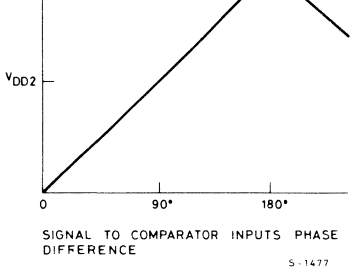


Fig. (b) - Typical waveforms for COS/MOS Phase-Locked-Loop employing phase comparator I in locked condition of f_o

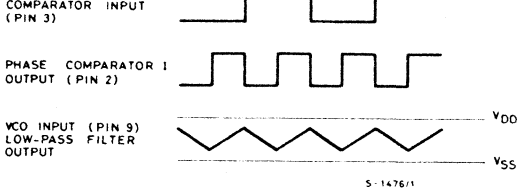
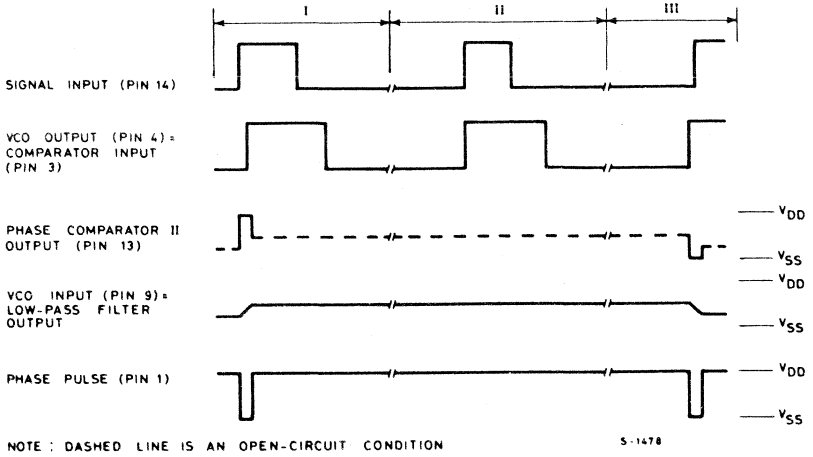


Fig.(c) - Typical waveforms for COS/MOS Phase-Locked Loop employing phase comparator II in locked condition



ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

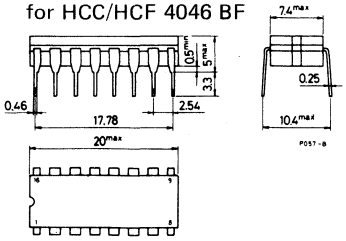
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

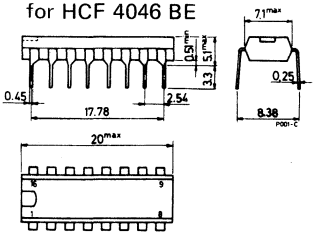
HCC 4046 BD for dual in-line ceramic package
HCC 4046 BF for dual in-line ceramic package, frit seal
HCC 4046 BK for ceramic flat package
HCF 4046 BE for dual in-line plastic package
HCF 4046 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

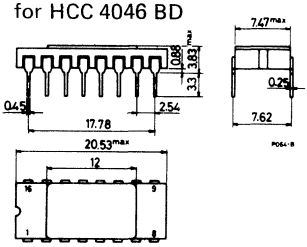
Dual in-line ceramic package for HCC/HCF 4046 BF



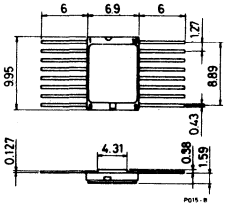
Dual in-line plastic package for HCF 4046 BE



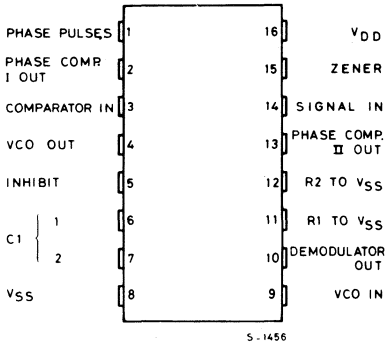
Dual in-line ceramic package for HCC 4046 BD



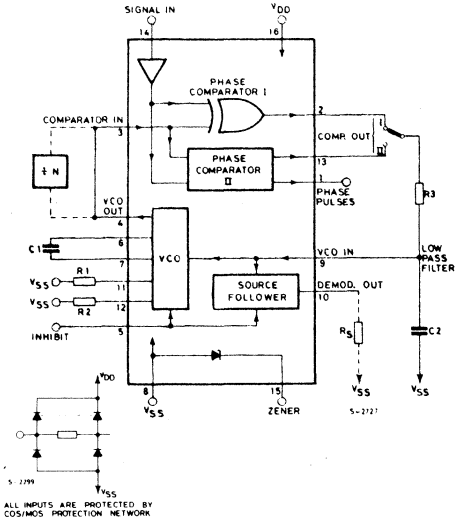
Ceramic flat package for HCC 4046 BK



CONNECTION DIAGRAM



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C)

Parameter		Test conditions		V_{DD}	Values Min.	Typ.	Max.	Unit
VCO Section								
P_D	Operating power dissipation	f_o= 10 KHz, R2= ∞	R1= 1 MΩ, $V_{COIN}=\frac{V_{DD}}{2}$	5		100		μW
				10		700		
				15		3000		
f_{max}	Maximum frequency	R1= 5 KΩ, R2= ∞, $V_{COIN}=V_{DD}$	C1= 50 pF	5		0.7		MHz
				10		1.4		
				15		1.9		
	Center frequency (f_o) and frequency range f_{max}-f_{min}	Programmable with external components R1, R2 and C1						
	Linearity	$V_{COIN}=2.5V^{\pm 0.3}$	R1 > 10 kΩ	5		1		%
		$V_{COIN}=5V^{\pm 2.5}$	R1 > 400 kΩ	10		1		
		$V_{COIN}=7.5V^{\pm 5}$	R1= 1 MΩ	15		1		
	Temperature frequency stability (no frequency offset) f_{min}= 0	$\%/°C \propto \frac{1}{f \cdot V_{DD}}$, R2= ∞		5		0.12-0.24		%/°C
				10		0.04-0.08		
				15		0.015-0.03		
	Frequency offset $f_{min} \neq 0$	$\%/°C \propto \frac{1}{f \cdot V_{DD}}$		5		0.06-0.12		
				10		0.05-0.1		
				15		0.03-0.06		
R_I	Input resistance of V_{COIN} (Pin 9)			5, 10, 15		10^{12}		Ω
V_{OL}	VCO output voltage (Pin 4) low level			5, 10, 15			0.05	
V_{OH}	VCO output voltage (Pin 4) high level			5	4.95			V
				10	9.95			
				15	14.95			
V_{CO}	Output duty cycle			5, 10, 15		50		%
t_{THL}, t_{TLH}	VCO output transition time			5		100		ns
				10		50		
				15		40		
I_{DN}	VCO output drive current N-channel (sinck)		V_o= 0.4V	5	0.51	1		mA
			V_o= 0.5V	10	1.3	2.6		
			V_o= 1.5V	15	3.4	6.8		
I_{DP}	VCO output drive current P-channel (source)		V_o= 4.6V	5	-0.51	-1		
			V_o= 9.5V	10	-1.3	-2.6		
			V_o= 13.5V	15	-3.4	-6.8		
	Source follower output (demodulated output): offset voltage V_{COIN}-V_{DEM}	R_S > 10 kΩ		5, 10, 15		1.5		V
	Source follower output (demodulated output): Linearity	R_S > 50 kΩ	$V_{COIN}=2.5^{\pm 0.3}V$	5		0.1		%
			$V_{COIN}=5^{\pm 2.5}V$	10		0.6		
			$V_{COIN}=7.5^{\pm 5}V$	15		0.8		
V_Z	Zener diode voltage	I_Z= 50 μA				5.2		V
R_Z	Zener dynamic resistance	I_Z= 1 mA				50		Ω

ELECTRICAL CHARACTERISTICS (continued)

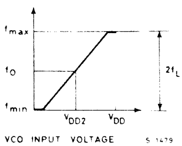
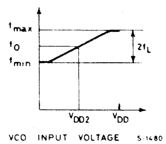
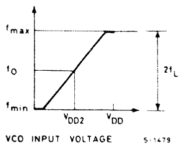
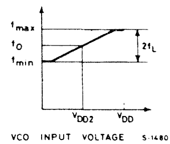
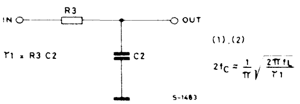
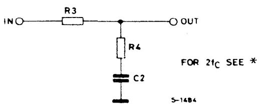
Parameter		Test conditions		V_{DD}	Values Min.	Typ.	Max.	Unit
PHASE COMPARATOR SECTION								
I_{DD}	Total quiescent device current (pin 14 open)	Pin 15 open		5		25		μA
				10		200		
				15		600		
I_{DD}	Total quiescent device current (pin 14 at V_{SS} or V_{DD})	Pin 5 at V_{DD} Pins 3 and 9 at V_{SS}		5		5		
				10		25		
				15		40		
				20		60		
R14	Pin 14 (signal in) input resistance			5		2		MΩ
				10		0.4		
				15		0.2		
	A.C. coupled signal input voltage sensitivity* (peak-to-peak)			5		200		mV
				10		400		
				15		700		
	D.C. coupled signal input and comparator input voltage sensitivity, low level			5	1.5	2.25		V
				10	3	4.5		
				15	4.5	6.75		
	D.C. coupled signal input and comparator input voltage sensitivity, high level			5		2.75	3.5	
				10		5.5	7	
				15		8.25	11	
I_{DN}	Output drive current N-channel (sink)	Phase comparator I and II (pin 2 and 13) and Phase Pulses	V_O= 0.4	5	0.51	1		mA
			V_O= 0.5	10	1.3	2.6		
			V_O= 1.5	15	3.4	6.8		
I_{DP}	Output drive current P-channel (source)	Phase comparator I and II (pin 2 and 13) and Phase Pulses	V_O= 4.6	5	-0.51	-1		
			V_O= 9.5	10	-1.3	-2.6		
			V_O= 13.5	15	-3.4	-6.8		
I_{IN}	Input current	Any input except pin 14		18		$\pm 10^{-5}$	± 0.1	μA
I_{OUT}	3-state output leakage current	pin 13	V_O= 0/18	18		$\pm 10^{-4}$		μA

* For sine wave, the frequency must be greater than 1 kHz for Phase Comparator II.

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the **HCC/HCF 4046B** in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

5 kΩ ⩽ R1, R2, R_S ⩽ 1 MΩ C1 ⩾ 100 pF at V_{DD} ⩾ 5V C1 ⩾ 50 pF at V_{DD} ⩾ 10V

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
VCO Frequency				
For No Signal Input	VCO in PLL system will adjust to centre frequency f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	$2f_L$ = full VCO frequency range $2f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2f_C$			$f_C = f_L$	
Loop Filter Component Selection				
Phase Angle between Signal and Comparator	90° at centre frequency (f_o), approximating 0° and 180° at ends of lock range ($2f_L$)		Always 0° in lock	
Locks on Harmonics of Centre Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	

* G.S. Mosckytz "miniaturized RC filters using phase Lockedloop" BSTJ, may 1965.

COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

LOW-POWER MONOSTABLE/ASTABLE MULTIVIBRATOR

- LOW POWER CONSUMPTION: SPECIAL COS/MOS OSCILLATOR CONFIGURATION
- MONOSTABLE (ONE-SHOT) OR ASTABLE (FREE-RUNNING) OPERATION
- TRUE AND COMPLEMENTED BUFFERED OUTPUTS
- ONLY ONE EXTERNAL R AND C REQUIRED
- BUFFERED INPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED, SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4047B** (extended temperature range) and **HCF 4047B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4047B** consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options. Inputs include +TRIGGER, - TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, $\overline{Q}$, and OSCILLATOR. In all modes of operation, an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals. For operating modes see functional terminal connections and application notes.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

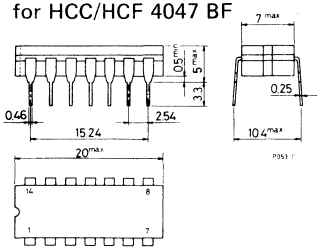
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

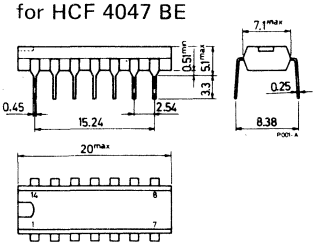
HCC 4047 BD for dual in-line ceramic package
HCC 4047 BF for dual in-line ceramic package, frit seal
HCC 4047 BK for ceramic flat package
HCF 4047 BE for dual in-line plastic package
HCF 4047 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

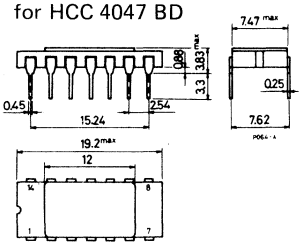
Dual in-line ceramic package
for HCC/HCF 4047 BF



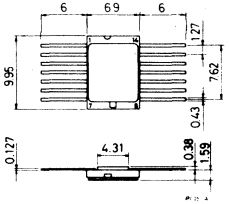
Dual in-line plastic package
for HCF 4047 BE



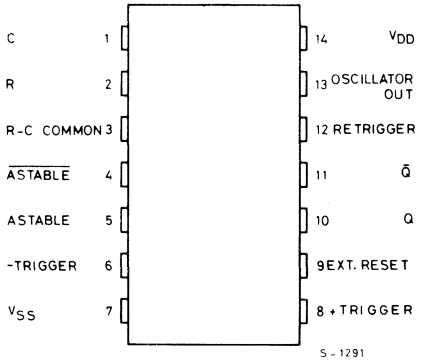
Dual in-line ceramic package
for HCC 4047 BD



Ceramic flat package
for HCC 4047 BK



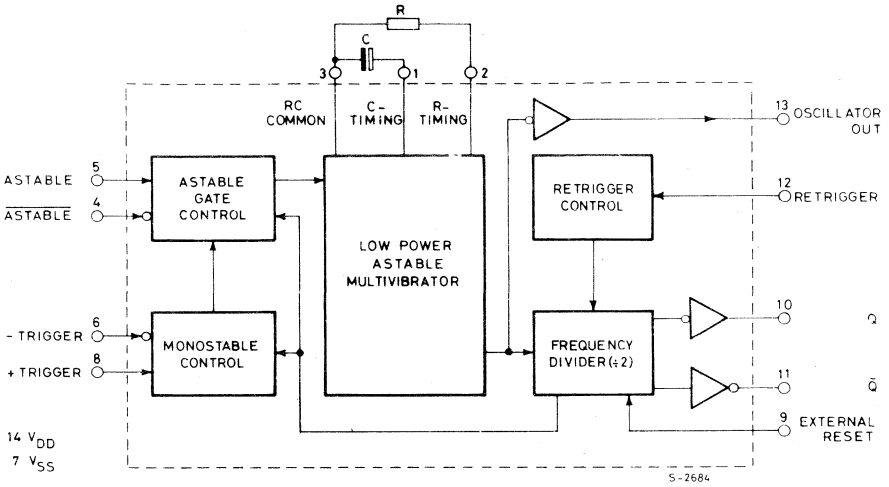
CONNECTION DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

BLOCK DIAGRAM



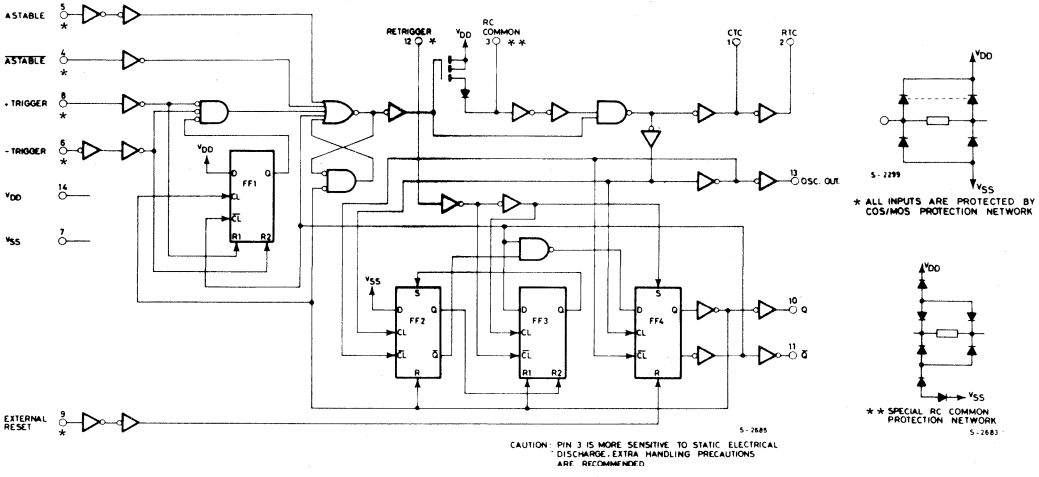
FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION*	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
Astable Multivibrator:					
Free Running	4, 5, 6, 14	7, 8, 9, 12	–	10, 11, 13	t_A (10, 11) = 4.40 RC
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	t_A (13) = 2.20 RC
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable Multivibrator:					
Positive-Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	t_M (10, 11) = 2.48 RC
External Countdown**	14	5, 6, 7, 8, 9, 12	–	10, 11	

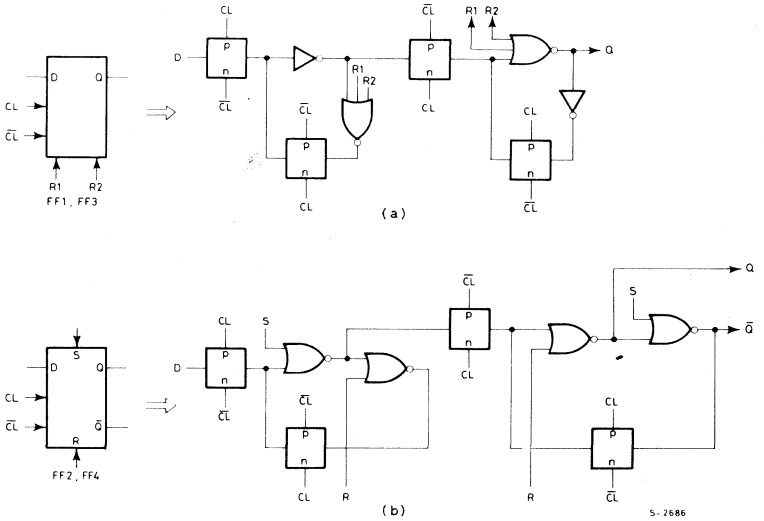
* In all cases external capacitor and resistor between pins, 1, 2 and 3 (see logic diagrams)

** Input pulse to Reset of External Counting Chip
External Counting Chip Output to pin 4

LOGIC DIAGRAMS



Detail for flip-flops FF1 and FF3 (a) and for flip-flops FF2 and FF4 (b)



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

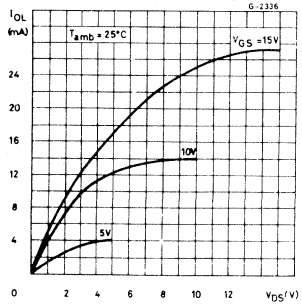
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

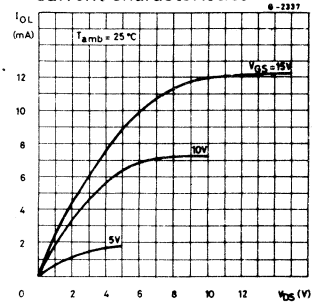
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 15 nF, R_L = 200 KΩ typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter			Test conditions	Values			Unit
				V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time	Astable, $\overline{\text{Astable}}$ to osc. out.		5		200		ns
				10		100		
				15		70		
		Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$		5		550		
				10		250		
				15		150		
		+Trigger, -Trigger to Q, $\overline{Q}$		5		700		
				10		300		
				15		200		
		+Trigger, Retrigger to Q, $\overline{Q}$		5		300		
				10		175		
				15		125		
		External Reset to Q, $\overline{Q}$		5		300		
				10		125		
				15		75		
t_{THL}, t_{TLH}	Transition time osc. out Q, $\overline{Q}$			5		100		ns
				10		50		
				15		40		
t_W	Input pulse width (any input)			5		500		ns
				10		200		
				15		140		
t_r, t_f	+Trigger, Retrigger rise and fall time			5		15		μs
				10		5		
				15		5		

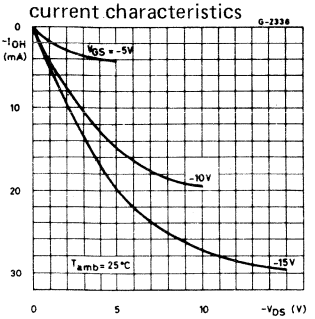
Typical output low (sink) current characteristics



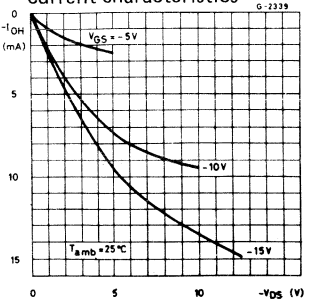
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics

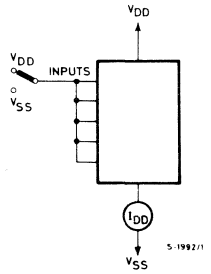


Minimum output high (source) current characteristics

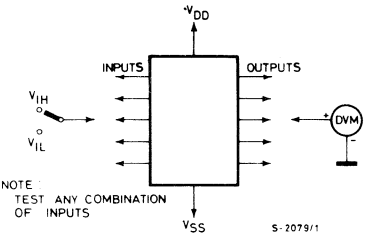


TEST CIRCUITS

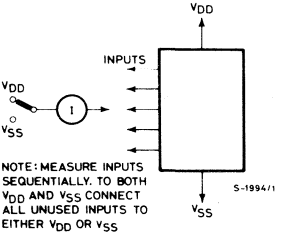
Quiescent device current



Input voltage



Input current



APPLICATION INFORMATION

1 - Circuit description

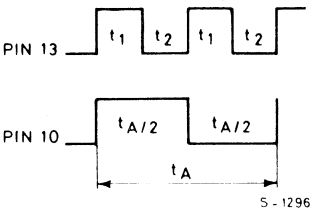
Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output. In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGGER input and a low level to the -TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the -TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the input pulse period is shorter than the period determined by the RC components. An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator. A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever V_{DD} is applied.

APPLICATION INFORMATION (continued)

2 - Astable Mode

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33% - 67% V_{DD}) for free-running (astable) operation.

Astable mode waveforms



$$t_1 = -RC \text{ in } \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \text{ in } \frac{V_{DD}-V_{TR}}{2\,V_{DD}-V_{TR}}$$

$$t_A = 2\,(t_1 + t_2) = -2\,RC \text{ in } \frac{(V_{TR})\,(V_{DD}-V_{TR})}{(V_{DD} + V_{TR})\,(2\,V_{DD} - V_{TR})}$$

Typ : $V_{TR} = 0.5\ V_{DD}$ $t_A = 4.40\ RC$
Min : $V_{TR} = 0.33\ V_{DD}$ $t_A = 4.62\ RC$
Max : $V_{TR} = 0.67\ V_{DD}$ $t_A = 4.62\ RC$

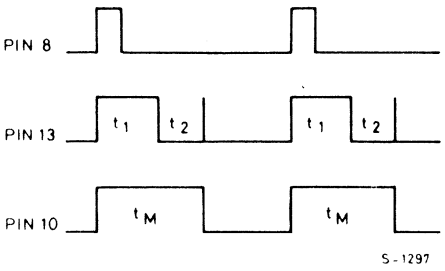
thus if $\boxed{t_A = 4.40\ RC}$ is used, the maximum variation will be (+5.0%, -0.0%)

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature.

3 - Monostable Mode

The following analysis presents worst-case variations from unit-to-unit as a function of transfer-voltage (V_{TR}) shift (33% - 67% V_{DD}) for one-shot (monostable) operation.

Monostable waveforms



$$t_1 = -RC \text{ in } \frac{V_{TR}}{2\,V_{DD}}$$

$$t_2 = -RC \text{ in } \frac{V_{DD}-V_{TR}}{2\,V_{DD}-V_{TR}}$$

$$t_M = (t_1 + t_2) = -RC \text{ in } \frac{(V_{TR})\,(V_{DD} - V_{TR})}{(2\,V_{DD} - V_{TR})\,(2\,V_{DD})}$$

APPLICATION INFORMATION (continued)

where t_M = monostable mode pulse width. Values for t_M are as follows:

Typ : $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48\ RC$
Min : $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71\ RC$
Max : $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48\ RC$

Thus if $\boxed{t_M = 2.48\ RC}$ is used, the maximum variation will be (+9.3%, -0.0%).

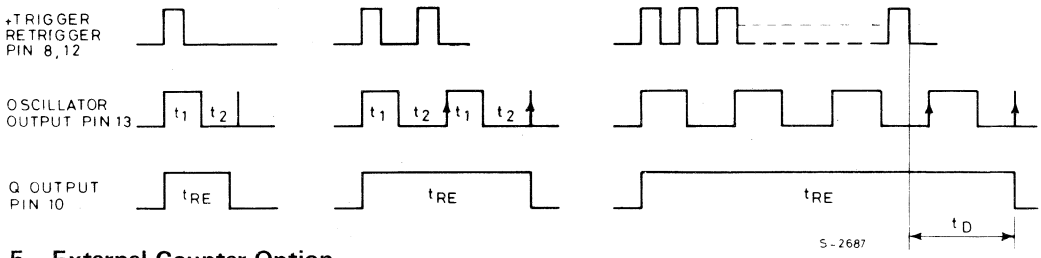
Note: In the astable mode, the first positive half cycle has a duration of T_M; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature.

4 - Retrigger Mode

The **HCC/HCF 4047B** can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig. A normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE} = t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (Q OUTPUT) terminates at some variable time t_D after the termination of the last retrigger pulse. t_D is variable because t_{RE} (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see logic diagram).

Fig. A - Retrigger-mode waveforms



5 - External Counter Option

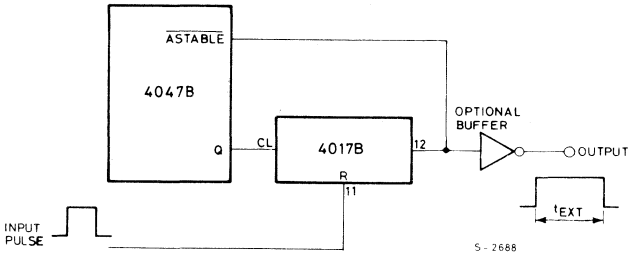
Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time.
A typical implementation is shown in Fig. B. The pulse duration at the output is

$$t_{ext} = (N - 1)\ (t_A) + (t_M + t_A/2)$$

where t_{ext} = pulse duration of the circuitry, and N is the number of counts used.

APPLICATION INFORMATION (continued)

Fig. B - Implementation of external counter option



6 - Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formula:

Astable Mode: $P = 2CV^2f$. (Output at Pin 13)
$P = 4CV^2f$. (Output at Pin 10 and 11)

Monostable Mode: $P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$

(Output at Pin 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.
Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above).

7 - Timing-component limitations

The capacitor used in the circuit should be non-polarized and have low leakage(i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). Three is no upper or lower limit for either R or C value to maintain oscillation.
However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the COS/MOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.
The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geqslant$ 100 pF, up to any practical value, for astable modes;
$C \geqslant 1000$ pF, up to any practical value, for monostable modes.
$10\ K\Omega \leqslant R \leqslant 1\ M\Omega$.

COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4048B

PRELIMINARY DATA

MULTIFUNCTION EXPANDABLE 8-INPUT GATE

- THREE-STATE OUTPUT
- MANY LOGIC FUNCTIONS AVAILABLE IN ONE PACKAGE
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4048B** (extended temperature range) and **HCF 4048B** (intermediate temperature range) are monolithic integrated circuit,available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4048B** is an 8-input gate having four control inputs. Three binary control inputs - Ka, Kb, and Kc - provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR. A fourth control input - Kd- provides the user with a 3-state output. When control input Kd is high the output is either a logic 1 or a logic 0 depending on the inner states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line. In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one **HCC/HCF 4048B**. For example, two **HCC/HCF 4048B**'s can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

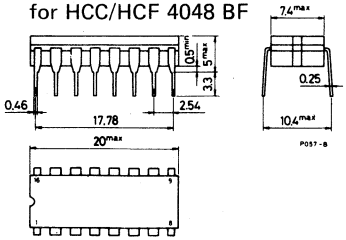
* All voltage values are referred to V_{SS} pin voltage

ORDERING BUMBERS:

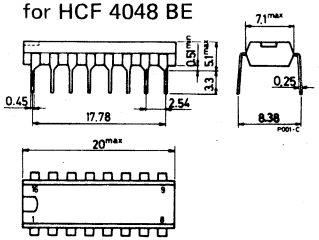
HCC 4048 BD for dual in-line ceramic package
HCC 4048 BF for dual in-line ceramic package, frit seal
HCC 4048 BK for ceramic flat package
HCF 4048 BE for dual in-line plastic package
HCF 4048 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

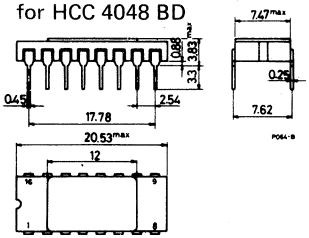
Dual in-line ceramic package for HCC/HCF 4048 BF



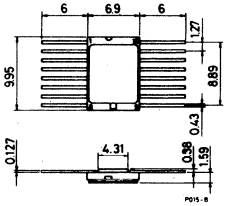
Dual in-line plastic package for HCF 4048 BE



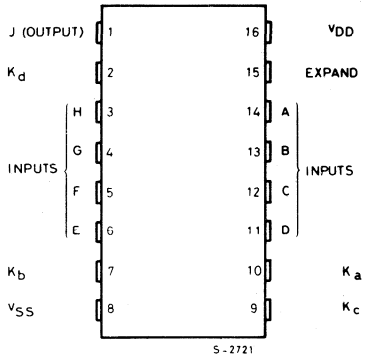
Dual in-line ceramic package for HCC 4048 BD



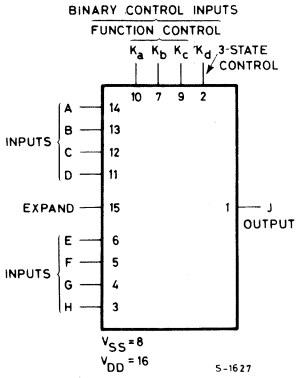
Ceramic flat package for HCC 4048 BK



CONNECTION DIAGRAM



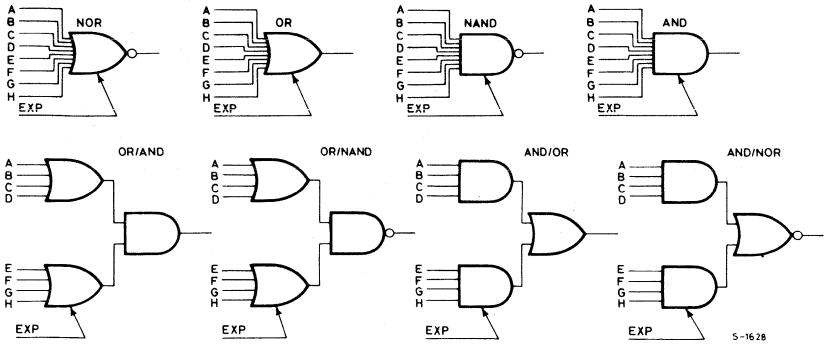
FUNCTIONAL DIAGRAM



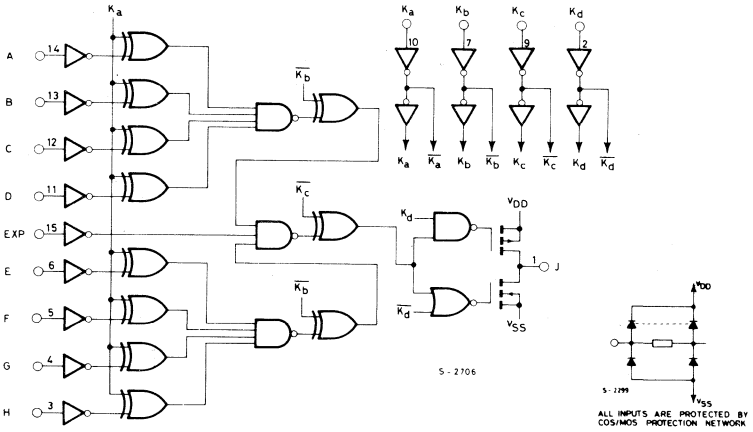
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

BASIC LOGIC CONFIGURATIONS



LOGID DIAGRAM



FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_a	K_b	K_c	UNUSED INPUT
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	$J=A+B+C+D+E+F+G+H$	0	0	1	V_{SS}
OR/AND	$J=(A+B+C+D)\cdot(E+F+G+H)$	0	1	0	V_{SS}
OR/NAND	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	$J=ABCDEFGH$	1	0	0	V_{DD}
NAND	$J=\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	$J=ABCD+EFGH$	1	1	1	V_{DD}

$K_d=1$ Normal Inverter Action
$K_d=0$ High Impedance Output

EXPAND Input = 0

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

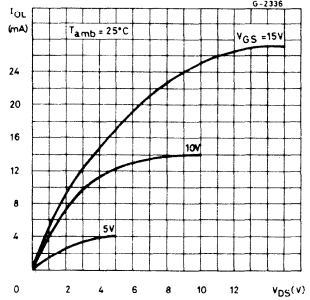
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				2/13	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13/2	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		± 0.1		±10^{-5}	± 0.1		± 1	μA
I_{OH}	3-state output current		0/18	0/18		18		± 0.4		±10^{-4}	± 0.4		± 12	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

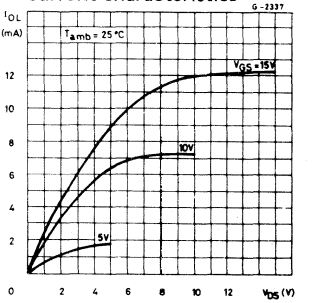
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time		5		300		ns
		10		130		
		15		100		
t_{TLH}, t_{THL} Transition time		5		100		ns
		10		50		
		15		40		

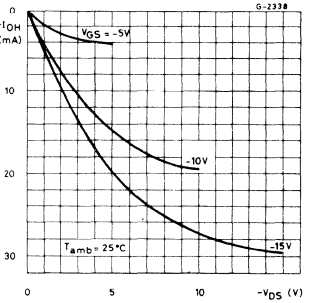
Typical output low (sink) current characteristics



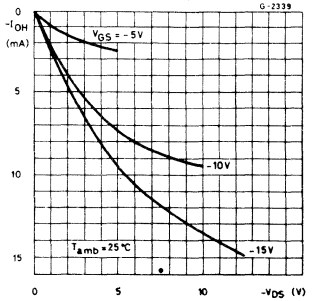
Minimum output low (sink) current characteristics



Typical output high (source) current characteristics

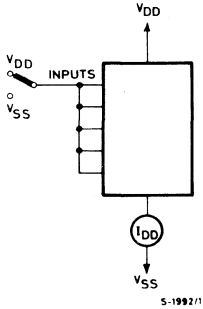


Minimum output high (source) current characteristics

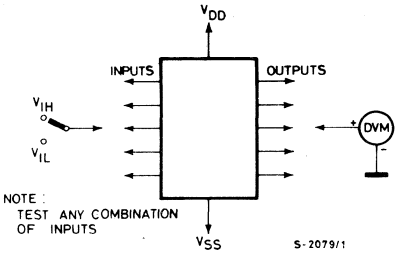


TEST CIRCUITS

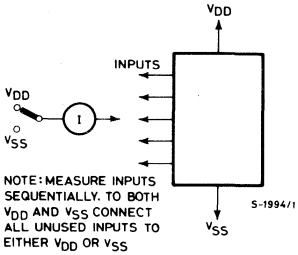
Quiescent device current



Input voltage

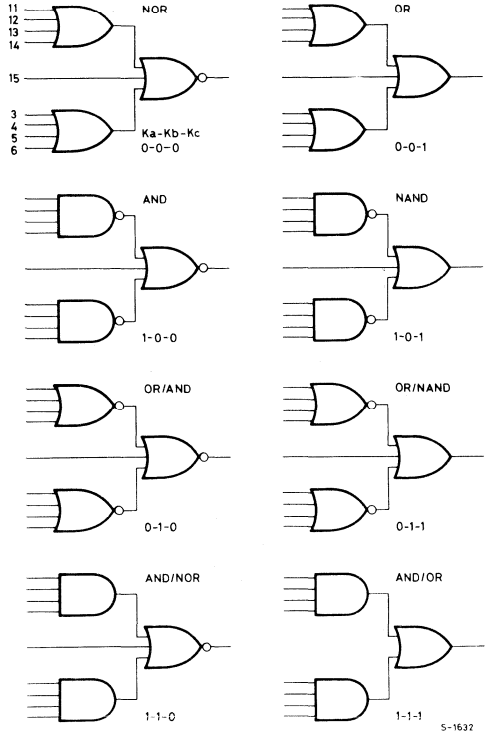


Input current



APPLICATIONS OF EXPAND INPUT

Actual-circuit logic configurations



Expansion logic and truth table

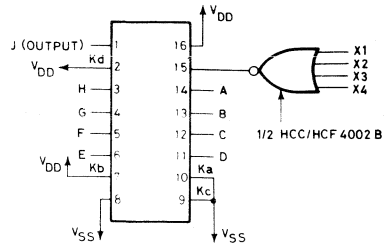
IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J = \overline{(A+B+C+D+E+F+G+H) + (EXP)}$
OR	OR	$J = (A+B+C+D+E+F+G+H) + (EXP)$
AND	NAND	$J = (ABCDEFGH) \cdot (EXP)$
NAND	NAND	$J = \overline{(ABCDEFGH) \cdot (EXP)}$
OR/AND	NOR	$J = \overline{(A+B+C+D) \cdot (E+F+G+H) \cdot (EXP)}$
OR/NAND	NOR	$J = (A+B+C+D) \cdot (E+F+G+H) \cdot (EXP)$
AND/NOR	AND	$J = \overline{(ABCD) + (EFGH) + (EXP)}$
AND/OR	AND	$J = (ABCD) + (EFGH) + (EXP)$

Note: (EXP) designates the EXPAND function (i.e., $X_1 + X_2 + \ldots X_N$)

APPLICATIONS (continued)

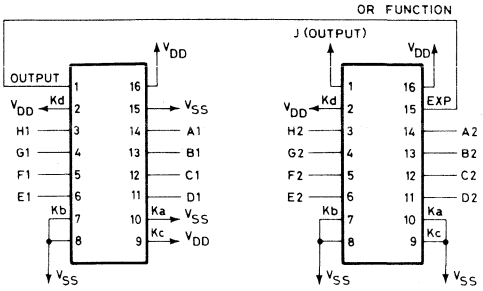
12-input OR/AND gate



12-INPUT OR/AND GATE
$J=(A\cdot B\cdot C\cdot D)\cdot(E+F+G+H)\cdot(X1+X2+X3+X4)$

S-2719

16-input NOR gate



16-INPUT NOR GATE

$\overline{J=A1\cdot B1\cdot C1\cdot D1\cdot E1\cdot F1\cdot G1\cdot H1\cdot A2\cdot B2\cdot C2\cdot D2\cdot E2\cdot F2\cdot G2\cdot H2}$

S-1631

PRELIMINARY DATA

HEX BUFFER/CONVERTERS: HCC/HCF 4049UB - INVERTING TYPE
HCC/HCF 4050B - NON-INVERTING TYPE

- HIGH SINK CURRENT FOR DRIVING 2 TTL LOADS
- HIGH-TO-LOW LEVEL LOGIC CONVERSION
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMP. RANGE)
- HIGH "SINK" AND "SOURCE" CURRENT CAPABILITY
- 5V, 10V AND 15V PARAMETRIC RATINGS

The **HCC 4049UB/4050B** (extended temperature range) and the **HCF 4049UB/4050B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4049UB/4050B** are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{DD}). The input-signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads (V_{DD}= 5V, $V_{OL} \leqslant 0.4V$, and $I_{OL} \geqslant 3.2$ mA).

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

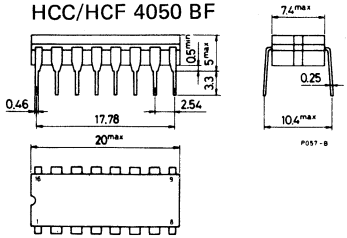
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

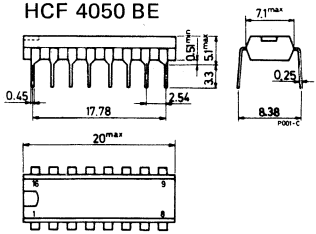
HCC 4049 UBD	for dual in-line ceramic package
HCC 4049 UBF	for dual in-line ceramic package, frit seal
HCC 4049 UBK	for ceramic flat package
HCF 4049 UBE	for dual in-line plastic package
HCF 4049 UBF	for dual in-line ceramic package, frit seal
HCC 4050 BD	for dual in-line ceramic package
HCC 4050 BF	for dual in-line ceramic package, frit seal
HCC 4050 BK	for ceramic flat package
HCF 4050 BE	for dual in-line plastic package
HCF 4050 BF	for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

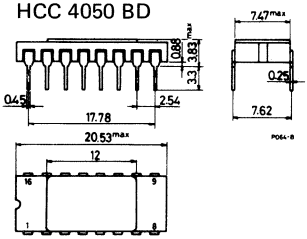
Dual in-line ceramic package for HCC/HCF 4049 UBF and HCC/HCF 4050 BF



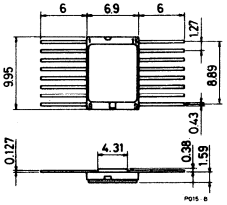
Dual in-line plastic package for HCF 4049 UBE and HCF 4050 BE



Dual in-line ceramic package for HCC 4049 UBD and HCC 4050 BD

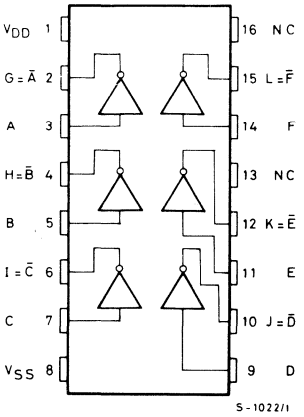


Ceramic flat package for HCC 4049 UBK and HCC 4050 BK

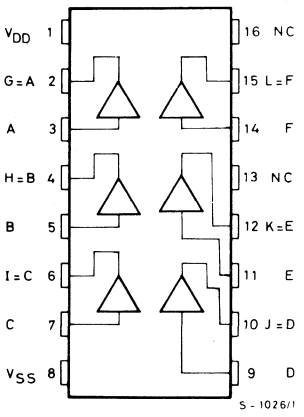


CONNECTION DIAGRAMS

For **4049 UB**



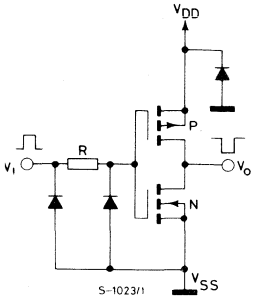
For **4050 B**



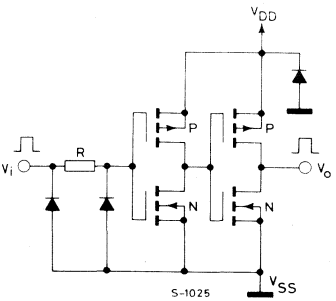
SCHEMATIC DIAGRAMS

1 of 6 identical units

For **4049 UB**

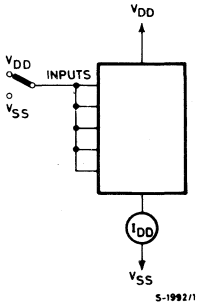


For **4050 B**

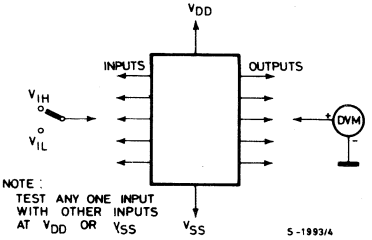


TEST CIRCUITS

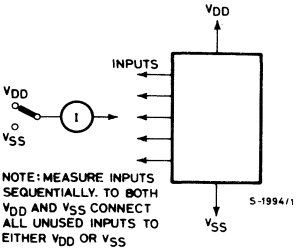
Quiescent device current



Input voltage



Input current



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

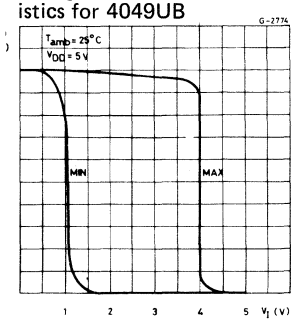
Parameter			Test conditions			Values							Unit
			V_I (V)	V_O (V)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
						Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5		5		1		0.02	1		30	μA
			0/10		10		2		0.02	2		60	
			0/15		15		4		0.02	4		120	
			0/20		20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		5	4.95		4.95			4.95		V
			0/10		10	9.95		9.95			9.95		
			0/15		15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		5		0.05			0.05		0.05	V
			10/0		10		0.05			0.05		0.05	
			15/0		15		0.05			0.05		0.05	
V_{IH}	Input high voltage (4049 UB)			0.5	5	4		4			4		V
				1	10	8		8			8		
				2	15	12		12			12		
V_{IH}	Input high voltage (4050 B)			4.5	5	3.5		3.5			3.5		V
				9	10	7		7			7		
				13.5	16	11		11			11		
V_{IL}	Input low voltage (4049 UB)			4.5	5		1			1		1	V
				9	10		2			2		2	
				13	15		3			3		3	
V_{IL}	Input low voltage (4050 B)			0.5	5		1.5			1.5		1.5	V
				1	10		3			3		3	
				1.5	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5	5	-4		-3.2	-6.4		-2.3		V
			0/ 5	4.6	5	-1		-0.8	-1.6		-0.6		
			0/10	9.5	10	-2.2		-1.8	-3.6		-1.3		
			0/15	13.5	15	-6.6		-6	-12		-4.4		
		HCF types	0/ 5	2.5	5	-3.6		-3.2	-6.4		-2.6		
			0/ 5	4.6	5	-0.9		-0.8	-1.6		-0.72		
			0/10	9.5	10	-2		-1.8	-3.6		-1.5		
			0/15	13.5	15	-6.4		-6	-12		-5		
I_{OL}	Output sink current	HCC types	0/ 5	0.4	4.5	3.3		2.6	5.2		1.8		V
			0/ 5	0.4	5	4		3.2	6.4		2.4		
			0/10	0.5	10	10		8	16		5.6		
			0/15	1.5	15	26		24	48		18		
		HCF types	0/ 5	0.4	4.5	3.1		2.6	5.2		2.1		
			0/ 5	0.4	5	3.8		3.2	6.4		2.9		
			0/10	0.5	10	9.6		8	16		6.6		
			0/15	1.5	15	24		24	48		20		
I_{IH},I_{IL}	Input leakage current		0/18	Any input	18		± 0.1		± 10^{-5}	± 0.1		± 1	μA
C_I	Input capacitance	4049UB	Any input						15	22.5			pF
		4050B							5	7.5			

* T_{Low} = − 55°C for **HCC** device; − 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin (only **HCC/HCF 4050B** type) for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

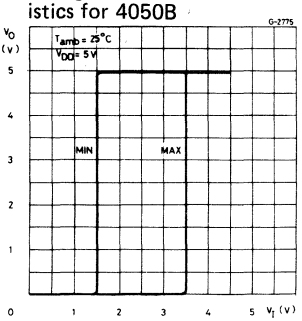
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

	Parameter	Test conditions		Values			Unit
		V_I(V)	V_{DD}(V)	Min.	Typ.	Max.	
t_{PLH}	Propagation delay time (4049 UB)	5	5		60	120	ns
		10	10		32	65	
		10	5		45	90	
		15	15		25	50	
		15	5		45	90	
t_{PLH}	Propagation delay time (4050 B)	5	5		70	140	ns
		10	10		40	80	
		10	5		45	90	
		15	15		30	60	
		15	5		40	80	
t_{PHL}	Propagation delay time (4049 UB)	5	5		32	65	
		10	10		20	40	
		10	5		15	30	
		15	15		15	30	
		15	5		10	20	
t_{PHL}	Propagation delay time (4050B)	5	5		55	110	ns
		10	10		22	55	
		10	5		50	100	
		15	15		15	30	
		15	5		50	100	
t_{TLH}	Transition time	5	5		80	160	ns
		10	10		40	80	
		15	15		30	60	
t_{THL}	Transition time	5	5		30	60	
		10	10		20	40	
		15	15		15	30	

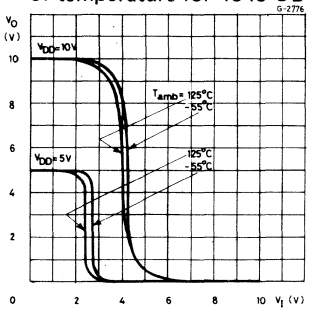
Minimum and maximum voltage transfer characteristics for 4049UB



Minimum and maximum voltage transfer characteristics for 4050B

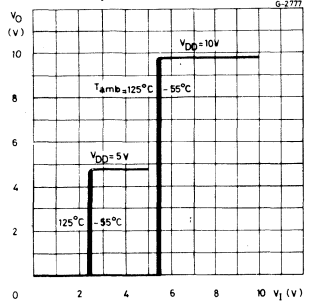


Typical voltage transfer characteristics as a function of temperature for 4049 UB

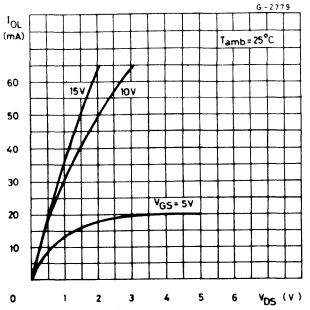


HCC/HCF 4049 UB
HCC/HCF 4050 B

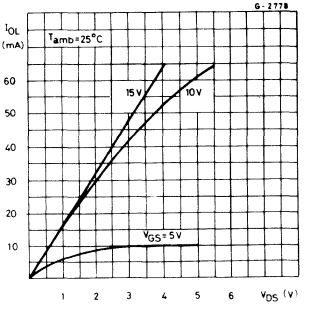
Typical voltage transfer characteristics as a function of temperature for 4050 B



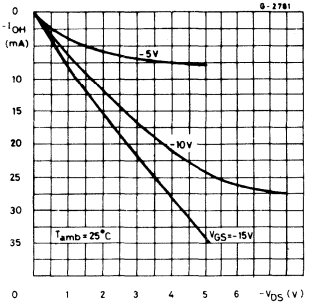
Typical output low (sink) current characteristics



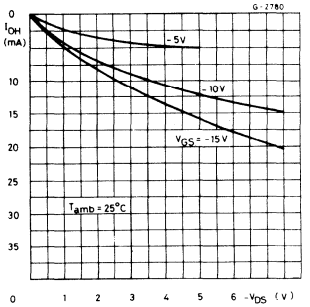
Minimum output low (sink) current drain characteristics



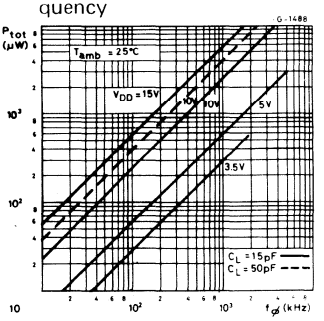
Typical output high (source) current characteristics



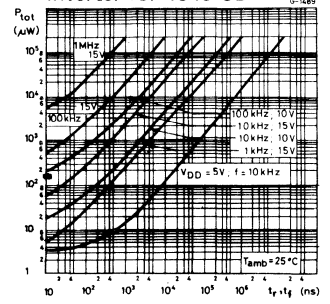
Minimum output high (source) current characteristics



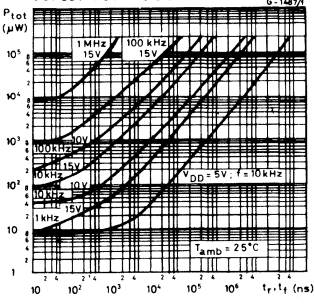
Typical power dissipation per buffer/inverter vs. frequency



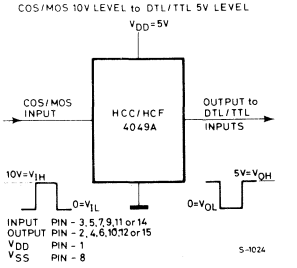
Typical power dissipation vs. input transition time per inverter for 4049 UB



Typical power dissipation vs. input transition time per inverter for 4050 B



Logic-level conversion application



COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

ANALOG MULTIPLEXERS-DEMULTIPLEXERS:
4051B - SINGLE 8-CHANNEL
4052B - DIFFERENTIAL 4-CHANNEL
4053B - TRIPLE 2-CHANNEL

- QUIESCENT CURRENT SPECIFIED TO 20V
- MAX. INPUT LEAKAGE CURRENT 1 μA @ 18V (FULL TEMP. RANGE)
- LOW"ON" RESISTANCE: 125Ω (TYP.) OVER 15V p.p. SIGNAL-INPUT RANGE for V_{DD}-V_{EE}= 15V
- HIGH"OFF" RESISTANCE: CHANNEL LEAKAGE ±100 pA (TYP.) V_{DD}-V_{EE}= 18V
- BINARY ADDRESS DECODING ON CHIP
- VERY LOW QUIESCENT POWER DISSIPATION UNDER ALL DIGITAL CONTROL INPUT and SUPPLY CONDITIONS: 0.2 μW (TYP.), V_{DD}-V_{SS}= V_{DD}-V_{EE}= 10V
- MATCHED SWITCH CHARACTERISTICS: R_{ON}= 5Ω (TYP.) for V_{DD}-V_{EE}= 15V
- WIDE RANGE OF DIGITAL AND ANALOG SIGNAL LEVELS: DIGITAL 3 TO 20V, ANALOG TO 20V p.p.
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4051B, 4052B** and **4053B** (extended temperature range) and **HCF 4051B, 4052B** and **4053B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. **HCC/HCF 4051B, HCC/HCF 4052B,** and **HCC/HCF 4053B** analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are off.

The **HCC/HCF 4051B** is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The **HCC/HCF 4052B** is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The **HCC/HCF 4053B** is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a singlepole double-throw configuration.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

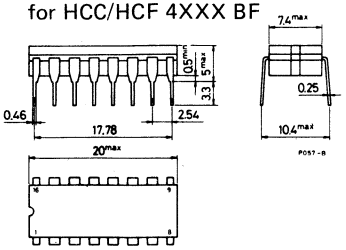
ORDERING NUMBERS:

HCC 4XXX	BD	for dual in-line ceramic package
HCC 4XXX	BF	for dual in-line ceramic package, frit seal
HCC 4XXX	BK	for ceramic flat package
HCF 4XXX	BE	for dual in-line plastic package
HCF 4XXX	BF	for dual in-line ceramic package, frit seal

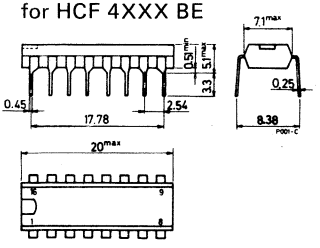
HCC/HCF 4051 B
HCC/HCF 4052 B
HCC/HCF 4053 B

MECHANICAL DATA (dimensions in mm)

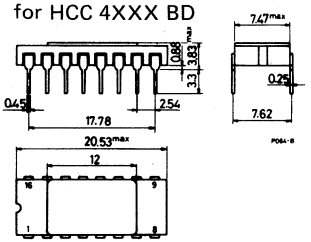
Dual in-line ceramic package
for HCC/HCF 4XXX BF



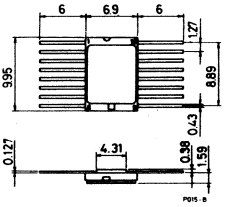
Dual in-line plastic package
for HCF 4XXX BE



Dual in-line ceramic package
for HCC 4XXX BD

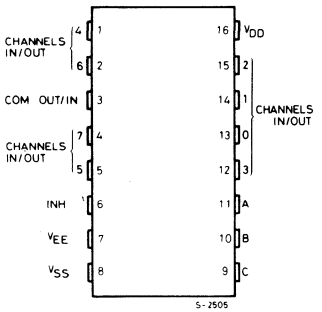


Ceramic flat package
for HCC 4XXX BK

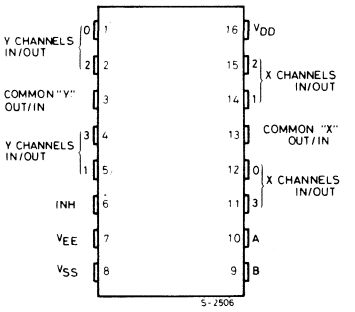


CONNECTION DIAGRAMS

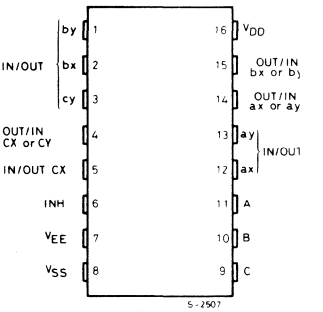
for **4051B**



for **4052B**



for **4053B**

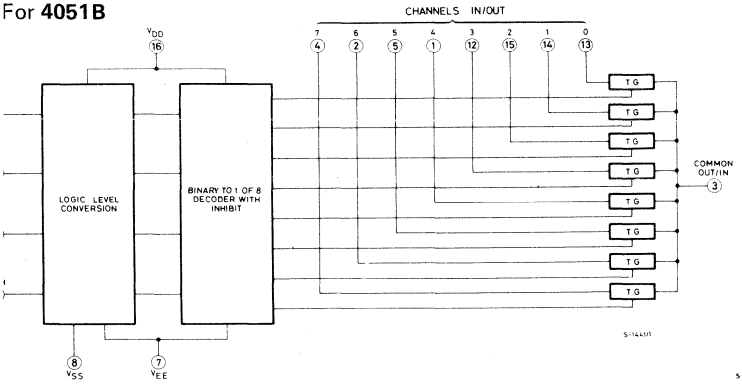


RECOMMENDED OPERATING CONDITIONS

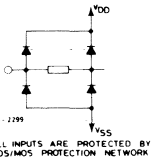
V_{DD}	Supply voltage	3 to 18	V
V_i	Input voltage	0 to V_{DD}	V
I_c	Multiplexer switch input current capability	25	mA
R_L	Minimum output load resistance	100	Ω
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

FUNCTIONAL DIAGRAMS AND TRUTH TABLES

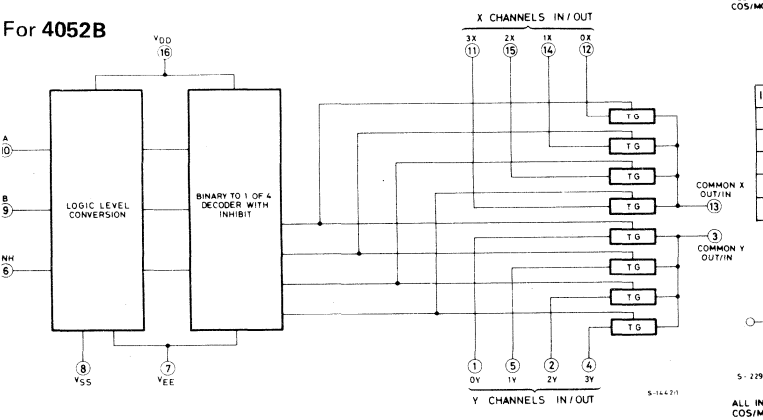
For **4051B**



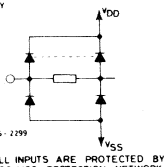
INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE



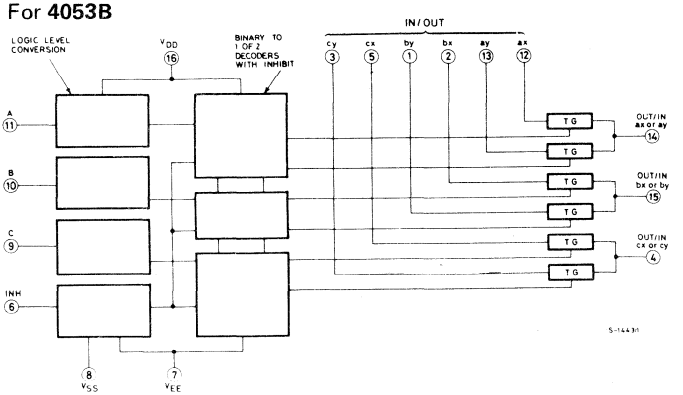
For **4052B**



INHIBIT	B	A	
0	0	0	0x, 0y
0	0	1	1x, 1y
0	1	0	2x, 2y
0	1	1	3x, 3y
1	X	X	NONE

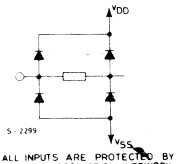


For **4053B**



INHIBIT	A or B or C	
0	0	ax or bx or cx
0	1	ay or by or cy
1	X	NONE

X = Don't care.



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	T_{Low} (*)		25°C			T_{High} (*)		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent device current					5		5		0.04	5		150	μA
						10		10		0.04	10		300	
						15		20		0.04	20		600	
						20		100		0.08	100		3000	
SWITCH														
ON	Resistance	HCC	$0 \leqslant V_I \leqslant V_{DD}$	0	0	5		2000		470	2500		3500	Ω
						10		310		180	400		580	
						15		220		125	280		400	
		HCF	$0 \leqslant V_I \leqslant V_{DD}$	0	0	5		2100		470	2500		3200	
						10		330		180	400		520	
						15		230		125	280		360	
ΔON	Resistance ΔR_{ON} (Between any 2 channels)			0	0	5				10				Ω
						10				10				
						15				5				
OFF	Channel(•) Leakage current	Any channel OFF		0	0	10		± 200		±0.01	± 200		± 200	nA
						15		± 500		±0.01	± 200		± 500	
						20		±1000		±0.01	± 200		±1000	
		All channels OFF (common OUT/IN)		0	0	10		± 200		±0.01	± 200		± 200	nA
						15		± 500		±0.01	± 200		± 500	
						20		±1000		±0.01	± 200		±1000	
C	Capacitance	Input		-5	-5	5				5				pF
		Output 4051								30				
		Output 4052								18				
		Output 4053								9				
		Feedthrough								0.2				
CONTROL (Address or Inhibit)														
V_{IL}	Input low voltage		= V_{DD} thru 1 KΩ	V_{EE}= V_{SS} R_L= 1 KΩ to V_{SS} I_{IS}< 2 μA (on all OFF channels)		5		1.5			1.5		1.5	V
						10		3			3		3	
						15		4			4		4	
V_{IH}	Input high voltage					5	3.5		3.5			3.5		V
						10	7		7			7		
						15	11		11			11		
I_{IH}, I_{IL}	Input leakage current		V_I= 0/18V			18		± 0.1		$±10^{-5}$	± 0.1		± 1	μA
C_i	Input capacitance		Any address or inhibit input							5	7.5			pF

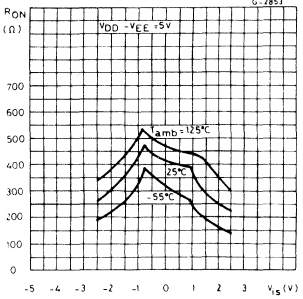
(•) Determined by minimum feasible leakage measurement for automatic testing.
(*) T_{Low} = − 55°C for HCC device; −40°C for HCF device.
T_{High} = +125°C for HCC device; +85°C for HCF device.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF all input square wave rise and fall times = 20 ns)

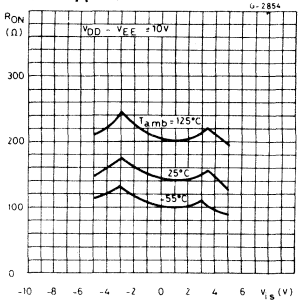
Parameter	Test conditions								Values		Unit
	V_{EE} (V)	R_L (kΩ)	f_i (KHz)	V_{IS} (V)	V_{SS} (V)	V_{DD} (V)			Typ.	Max.	
SWITCH											
t_{pd} Propagation delay time (Signal Input to output)		10		10V		5			30		ns
						10			15		
						15			11		
Frequency Response Channel "ON"(Sine Wave Input) at 20 Log $\frac{V_O}{V_I}$ = -3dB	$=V_{SS}$	1		5(•)		10	V_O at Common OUT/IN	4053B	30		MHz
								4052B	25		
								4051B	20		
							V_O at Any Channel		60		
Feedthrough (All channels OFF) at 20 Log $\frac{V_O}{V_I}$ = -40 dB	$=V_{SS}$	1		5(•)		10	V_O at Common OUT/IN	4053	8		MHz
								4052	10		
								4051	12		
							V_O at Any channel		8		
Frequency Signal Crosstalk at 20 Log $\frac{V_O}{V_I}$ = -40 dB	$=V_{SS}$	1		5(•)		10	Between Any 2 channels		3		MHz
							Between sections 4052B only	Measured on common	6		
								Measured on Any channel	10		
							Between Any 2 sections 4053B only	In Pin 2 Out Pin 14	2.5		MHz
								In Pin 15 Out Pin 14	6		
Sine wave Distortion	$=V_{SS}$	10	1	2(•)		5			0.3		%
		10	1	3(•)		10			0.2		
		10	1	5(•)		15			0.12		
CONTROL (Address or Inhibit)											
Propagation delay time: Address - to Signal OUT Channels ON or OFF	0				0	5			360	720	ns
	0				0	10			160	320	
	0				0	15			120	240	
	-5				0	5			225	450	
Propagation delay time: Inhibit to signal OUT (channel turning ON)	0	10			0	5			360	720	ns
	0				0	10			160	320	
	0				0	15			120	240	
	-10				0	5			200	400	
Propagation delay time: Inhibit to signal OUT (channel turning OFF)	0	0.3				5			200	450	ns
	0					10			90	210	
	0					15			70	160	
	-10					5			130	300	
Address or Inhibit to Signal Crosstalk	0	10*			0	10	$V_C=V_{DD}-V_{SS}$ (Square Wave)		65		mV peak

(•) Peak to peak voltage symmetrical about $\frac{V_{DD}-V_{EE}}{2}$
(*) Both ends of channel.

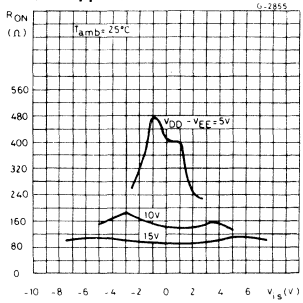
Typical channel ON resistance vs. input signal voltage (all types)



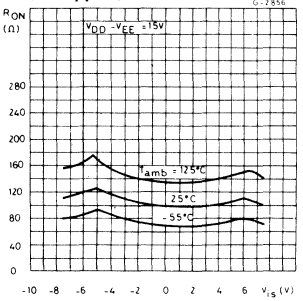
Typical channel ON resistance vs. input signal voltage (all types)



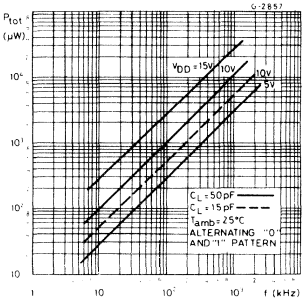
Typical channel ON resistance vs. input signal voltage (all types)

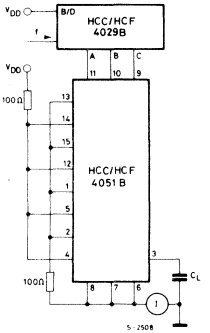


Typical channel ON resistance vs. input signal voltage (all types)

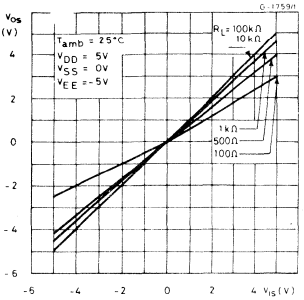


Typical dynamic power dissipation/package vs. switching frequency and test circuit (4051B)

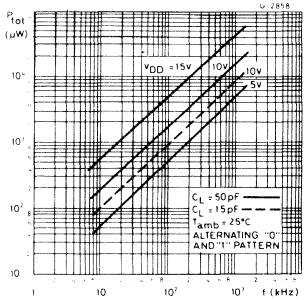


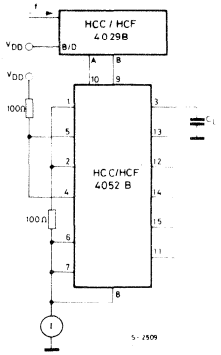


Typical ON characteristics for 1 of 8 channels (4051B)

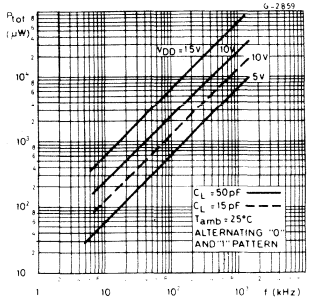


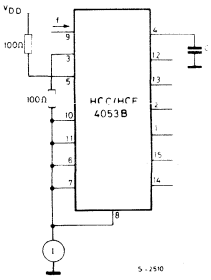
Typical dynamic power dissipation/package vs. switching frequency and test circuit (4052B)





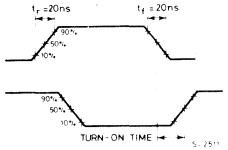
Typical dynamic power dissipation/package vs. switching frequency and test circuit (4053B)



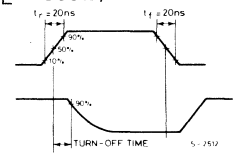


WAVEFORMS

Channel being turned ON (R_L = 10 KΩ)

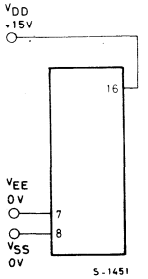


Channel being turned OFF (R_L = 300Ω)



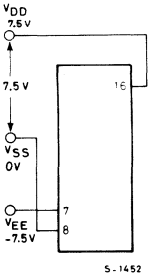
TYPICAL BIAS VOLTAGES

fig. (a)



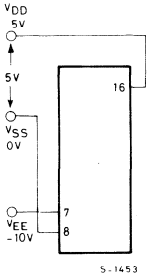
S-1451

fig. (b)



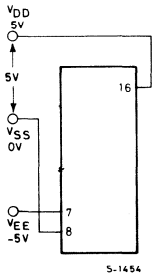
S-1452

fig. (c)



S-1453

fig. (d)



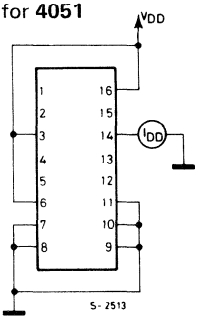
S-1454

The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = V_{SS} and "1" = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

TEST CIRCUITS

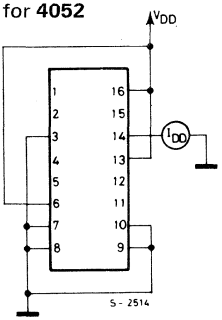
OFF channel leakage current-any channel OFF

for **4051**



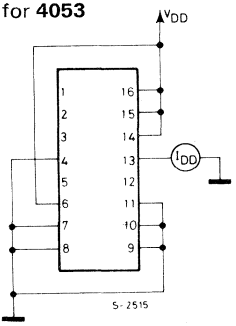
S-2513

for **4052**



S-2514

for **4053**

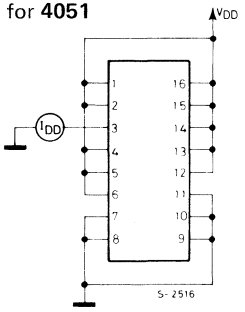


S-2515

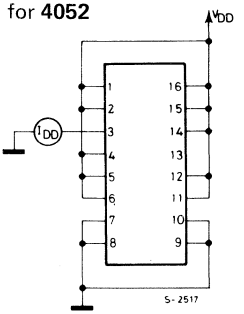
TEST CIRCUITS (continued)

OFF channel leakage current - all channel OFF

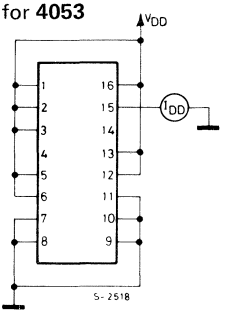
for **4051**



for **4052**

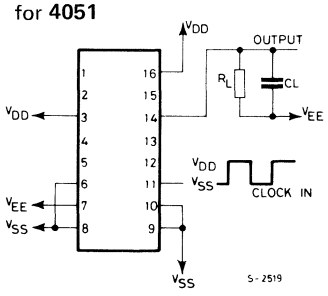


for **4053**

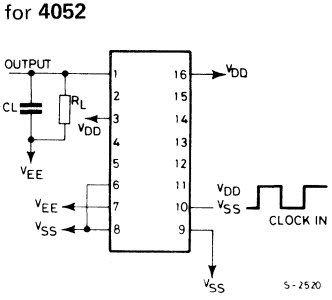


Propagation delay - address input to signal output

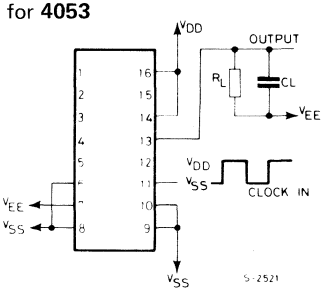
for **4051**



for **4052**

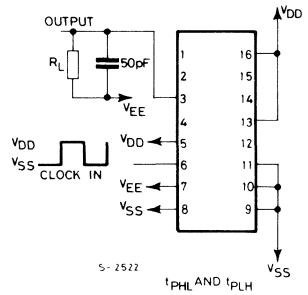


for **4053**

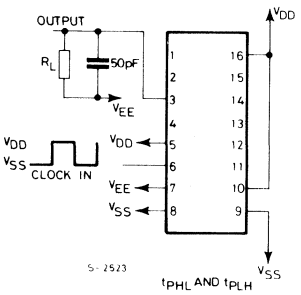


Propagation delay-inhibit input to signal output

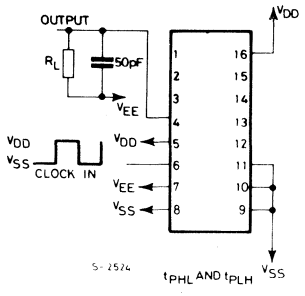
for **4051**



for **4052**



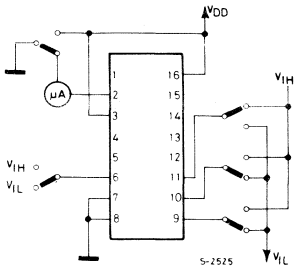
for **4053**



TEST CIRCUITS (continued)

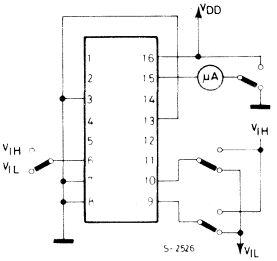
Input voltage

for **4051**



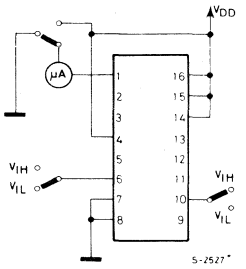
MEASURE < 2 μA ON ALL "OFF" CHANNELS (e.g. CHANNEL 6)

for **4052**



MEASURE < 2 μA ON ALL "OFF" CHANNELS (e.g. CHANNEL 2x)

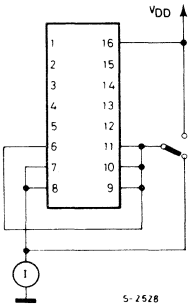
for **4053**



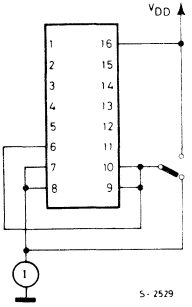
MEASURE 2 μA ON ALL "OFF" CHANNELS (e.g. CHANNEL by)

Quiescent device currrent

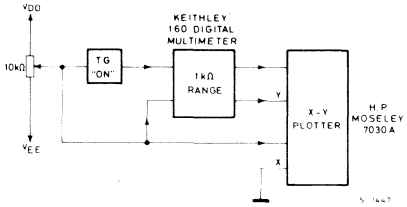
for **4051**
4053



for **4052**

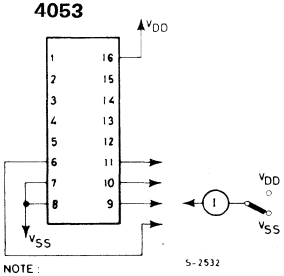


Channel ON resistance measurement circuit



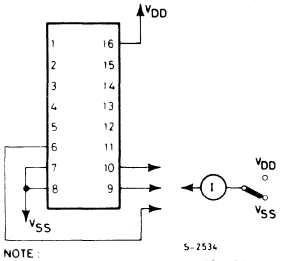
Input current

for **4051**
4053



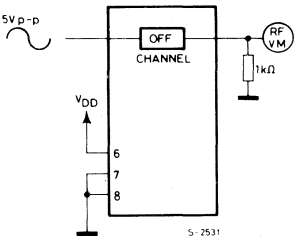
NOTE:
MEASURE INPUTS SEQUENTIALLY, TO BOTH V_{DD} AND V_{SS}. CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}.

for **4052**



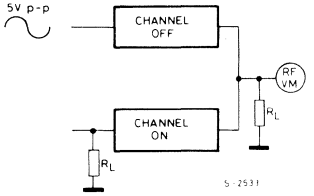
NOTE:
MEASURE INPUTS SEQUENTIALLY, TO BOTH V_{DD} AND V_{SS}. CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}.

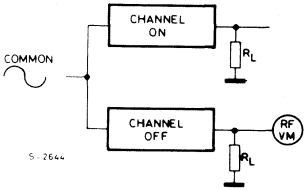
Feedthrough (all types)



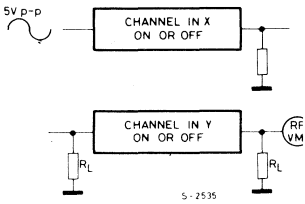
TEST CIRCUITS (continued)

Crosstalk between any two channels (all types)



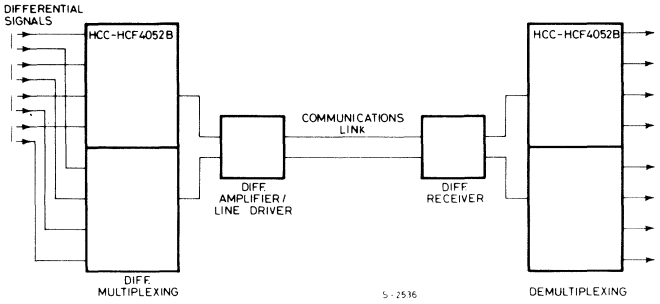


Crosstalk between duals or triplets (4052-4053)



TYPICAL APPLICATIONS

Typical time-division application of the 4052B



SPECIAL CONSIDERATIONS

Control of analog signals up to 20V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if V_{DD}-V_{SS}= 3V, a V_{DD}-V_{EE} of up to 13V can be controlled; for V_{DD}-V_{EE} level differences above 13V, a V_{DD}-V_{SS} of at least 4.5V is required). For example, if V_{DD}= +5V, V_{SS}= 0, and V_{EE}= -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0 to 4.5V. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0,8 volt (valvulated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into lead 3 on the **HCC/HCF 4051**; leads 3 and 13 on the **HCC/HCF 4052**; leads 4, 14, and 15 on the **HCC/HCF 4053**.

COS/MOS INTEGRATED CIRCUITS

HCC/HCF 4054 B
HCC/HCF 4055 B
HCC/HCF 4056 B

PRELIMINARY DATA

LIQUID-CRYSTAL DISPLAY DRIVERS

4054B - 4-SEGMENT DISPLAY DRIVER - STROBED LATCH FUNCTION
4055B - BCD TO 7-SEGMENT DECODER/DRIVER, WITH "DISPLAY-FREQUENCY" OUTPUT
4056B - BCD TO 7-SEGMENT DECODER/DRIVER WITH STROBED LATCH FUNCTION

- QUIESCENT CURRENT SPECIFIED TO 20V
- MAX. INPUT LEAKAGE CURRENT 1 μA @ 18V (FULL TEMP. RANGE)
- OPERATION OF LIQUID CRYSTALS WITH COS/MOS CIRCUITS PROVIDES ULTRA-LOW-POWER DISPLAYS
- EQUIVALENT AC OUTPUT DRIVE FOR LIQUID-CRYSTAL DISPLAYS-NO EXTERNAL CAPACITOR REQUIRED
- VOLTAGE DOUBLING ACROSS DISPLAY [(V_{DD}-V_{EE}) = 18V)] RESULTS IN EFFECTIVE 36V (p-p) DRIVE ACROSS SELECTED DISPLAY SEGMENTS
- LOW-OR HIGH-OUTPUT LEVEL DC DRIVE FOR OTHER TYPES OF DISPLAYS
- ON-CHIP LOGIC-LEVEL CONVERSION FOR DIFFERENT INPUT AND OUTPUT-LEVEL SWINGS
- FULL DECODING OF ALL INPUT COMBINATIONS: "0-9, L, H, P, A-" AND BLANK POSITIONS

The **HCC 4054B, HCC 4055B** and **HCC 4056B** (extended temperature range) and the **HCF 4054B, HCF 4055B** and **HCF 4056B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package. The **HCC/HCF 4055B** and **HCC/HCF 4056B** types are single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings (V_{DD} to V_{SS}) to be the same as or different from the 7-segment output-signal swings (V_{DD}.to V_{EE}). For example, the BCD input-signal swings (V_{DD} to V_{SS}) may be as low as 0 to -3V, whereas the output-display drive-signal swing (V_{DD} to V_{EE}) may be from 0 to -5V. If V_{DD} to V_{EE} exceeds 15V, V_{DD} to V_{SS} should be at least 4V. The 7-segment outputs are controlled by the DISPLAY-FREQUENCY (DF) input which causes the selected segment outputs to be low, high, or a square-wave output (for liquid-crystal displays). When the DF input is low the output segments will be high when selected by the BCD inputs. When the DF input is high, the output segments will be low when selected by the BCD inputs. When a square-wave is present at the DF input, the selected segments will have a square-wave output that is 180° out of phase with the DF input. Those segments which are not selected will have a square-wave output that is in phase with the input. DF square-wave repetition rates for liquid-crystal displays usually range from 30 Hz (well above flicker rate) to 200 Hz (well below the upper limit of the liquid-crystal frequency response). The **HCC/HCF 4055B** provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The **HCC/HCF 4056B** provides a strobed-latch function at the BCD inputs. Decoding of all input combinations on the **HCC/HCF 4055B** and **HCC/HCF 4056B** provides displays of 0 to 9 as well as L, P, H, A, –, and a blank position. (See typical application for other letters). The **HCC/HCF 4054B** provides level shifting similar to the **HCC/HCF 4055B** and **HCC/HCF 4056B** independently strobed latches, and common DF control on 4 signal lines. The **HCC/HCF 4054B** is intended to provide drive-signal compatibility with the **HCC/HCF 4055B** and **HCC/HCF 4056B** 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any **HCC/HCF 4054B** output line by connecting the corresponding input and strobe lines to a low and high level, respectively. The **HCC/HCF 4054B** may also be utilized for logic-level "up conversion" or "down conversion". For example, input-signal swings (V_{DD} to V_{SS}) from +5 to 0V can be converted to output-signal swings (V_{DD} to V_{EE}) of +5 to -5V. The level-shifted function on all three types permits the use of different input-and output-signal swings. The input swings from a low level of V_{SS} to a high level of V_{DD} while the output swings from a low level of V_{EE} to the same high level of V_{DD}. Thus, the input and output swings can be selected independently of each other over a 3-to-18V range. V_{SS} may be connected to V_{EE} when no level-shift function is required. For the **HCC/HCF 4054B** and **HCC/HCF 4056B**, data are transferred from input to output by placing a high voltage level at the strobe input. A low voltage level at the strobe input latches the data input and the corresponding output

segments remain selected (or non-selected) while the strobe is low. Whenever the level-shifting function is required, the **HCC/HCF 4055B** can be used by itself to drive a liquid-crystal display (Fig. 10 and Fig. 12). The **HCC/HCF 4056B**, however, must be used together with a **HCC/HCF 4054B** to provide the common DF output (Fig. 14). The capability of extending the voltage swing on the negative end (this voltage cannot be extended on the positive end) can be used to advantage in the setup of Fig. 11. Fig. 9 is common to all three types.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

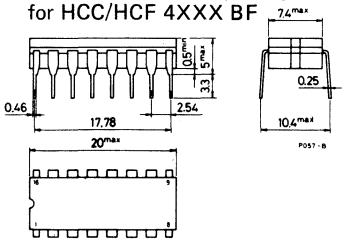
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

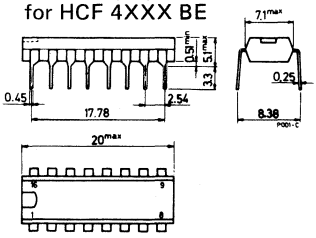
HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

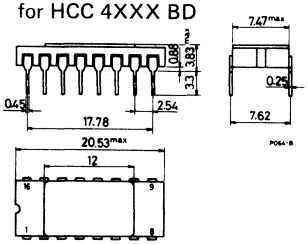
Dual in-line ceramic package for HCC/HCF 4XXX BF



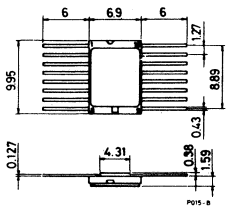
Dual in-line plastic package for HCF 4XXX BE



Dual in-line ceramic package for HCC 4XXX BD

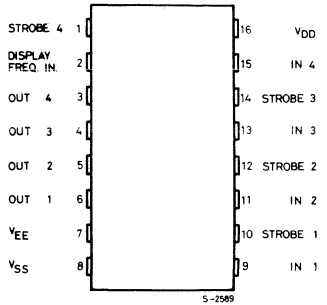


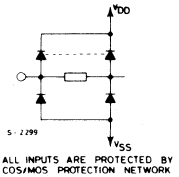
Ceramic flat package for HCC 4XXX BK



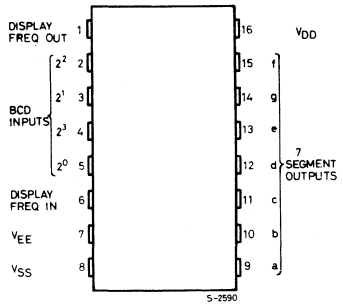
CONNECTION DIAGRAMS

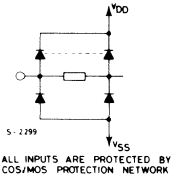
For 4054B



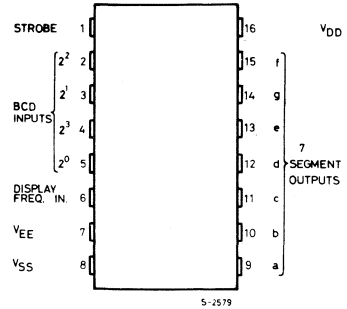


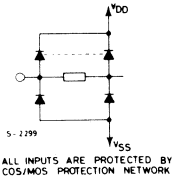
For 4055B





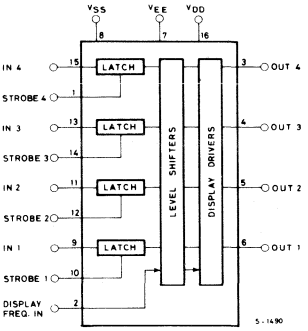
For 4056B



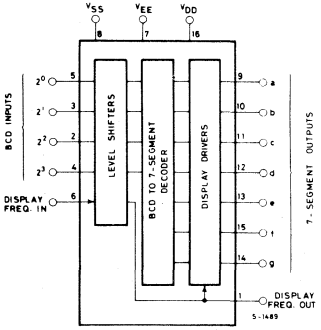


FUNCTIONAL DIAGRAMS

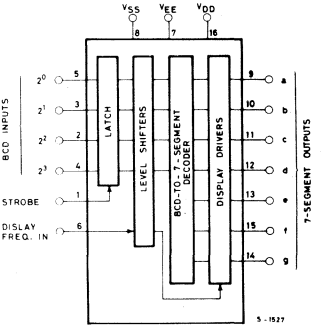
For 4054B



For 4055B



For 4056B



RECOMMENDED OPERATING CONDITIONS

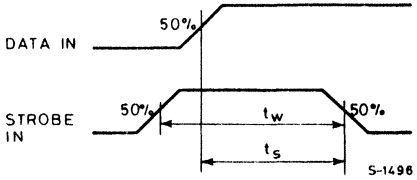
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

TRUTH TABLE

For **4055B** and **4056B**

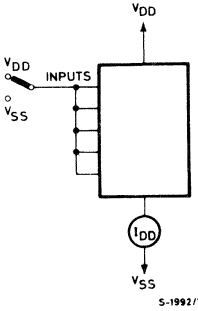
INPUT CODE				OUTPUT STATE							DISPLAY CHARACTER
2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	0	0	0	1	1	1	1	1	1	0	0
0	0	0	1	0	1	1	0	0	0	0	1
0	0	1	0	1	1	0	1	1	0	1	2
0	0	1	1	1	1	1	1	0	0	1	3
0	1	0	0	0	1	1	0	0	1	1	4
0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	0	1	1	1	1	1	6
0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	1	1	1	1	0	1	1	9
1	0	1	0	0	0	0	1	1	1	0	L
1	0	1	1	0	1	1	0	1	1	1	H
1	1	0	0	1	1	0	0	1	1	1	P
1	1	0	1	1	1	1	0	1	1	1	D
1	1	1	0	0	0	0	0	0	0	1	-
1	1	1	1	0	0	0	0	0	0	0	BLANK

Data setup time and strobe pulse duration

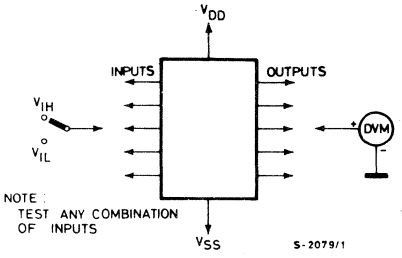


TEST CIRCUITS

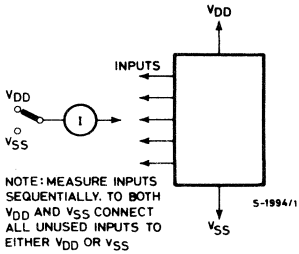
Quiescent device current



Input voltage



Input leakage current



STATIC ELECTRICAL CHARACTERISTICS (under recommended operating conditions)

Parameter			Test conditions					Values							Unit
			V_{EE} (V)	V_I (V)	V_O (V)	V_{SS} (V)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		-5	0/ 5		0	5		5		0.04	5		150	μA
			0	0/10		0	10		10		0.04	10		300	
			0	0/15		0	15		20		0.04	20		600	
			0	0/20		0	20		100		0.08	100		3000	
V_{OH}	Output high voltage		0	0/ 5		0	5	4.95		4.95			4.95		V
			0	0/10		0	10	9.95		9.95			9.95		
			0	0/15		0	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		0	5/0		0	5		0.05			0.05		0.05	V
			0	10/0		0	10		0.05			0.05		0.05	
			0	15/0		0	15		0.05			0.05		0.05	
V_{IH}	Input high voltage		-5		0.5/4.5	0	5	3.5		3.5			3.5		V
			0		1/9	0	10	7		7			7		
			0		2/13	0	15	11		11			11		
V_{IL}	Input low voltage		5		0.5/0.5	0	5		1.5			1.5		1.5	V
			0		9/1	0	10		3			3		3	
			0		2/13	0	15		4			4		4	
I_{OH}	Output high current	HCC types	-5	0/ 5	4.5	0	5	-0.6		-0.45	-0.9		-0.3		mA
			0	0/10	9.5	0	10	-0.6		-0.45	-0.9		-0.3		
			0	0/15	13.5	0	15	-1.9		-1.5	-3		-1.1		
		HCF types	-5	0/ 5	4.5	0	5	-0.55		-0.45	-0.9		-0.35		
			0	0/10	9.5	0	10	-0.55		-0.45	-0.9		-0.35		
			0	0/15	13.5	0	15	-1.8		-1.5	-3		-1.2		
I_{OL}	Output low current	HCC types	-5	0/ 5	0.4	0	5	1.6		1.3	2.6		0.9		mA
			0	0/10	0.5	0	10	1.6		1.3	2.6		0.9		
			0	0/15	1.5	0	15	4.2		3.4	6.8		2.4		
		HCF types	-5	0/ 5	0.4	0	5	1.5		1.3	2.6		1.1		
			0	0/10	0.5	0	10	1.5		1.3	2.6		1.1		
			0	0/15	1.5	0	15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0	0/18		0	18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
C_I**	Input capacitance										5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions				Types						Unit
		V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	4054B			4055B, 4056B			
					Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PHL}, t_{PLH} Propagation delay time (Any Input to Any output)		-5	0	5		400	800		650	1300	ns
		0	0	10		340	680		575	1150	
		0	0	15		250	500		375	750	
t_{THL}, t_{TLH} Transition time (Any output)		-5	0	5		100	200		100	200	ns
		0	0	10		100	200		100	200	
		0	0	15		75	150		75	150	
t_{setup}* Data setup time		-5	0	5	220	110		220	110		ns
		0	0	10	100	50		100	50		
		0	0	15	70	35		70	35		
t_W* Strobe pulse width		-5	0	5	220	110		220	110		ns
		0	0	10	100	50		100	50		
		0	0	15	70	35		70	35		

* HCC/HCF 4054B and HCC/HCF 4056B only.

Fig. 1 - Typical output low (sink) current characteristics

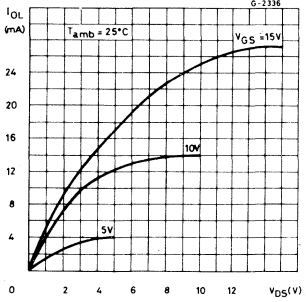


Fig. 2 - Minimum output low (sink) current characteristics

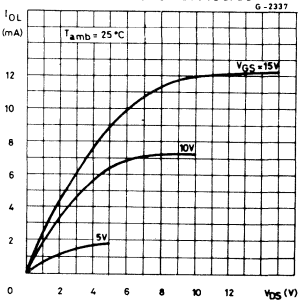


Fig. 3 - Typical output high (source) current characteristics

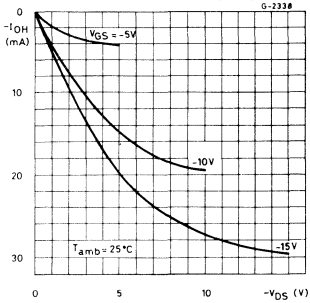


Fig. 4 - Minimum output (source) current characteristics

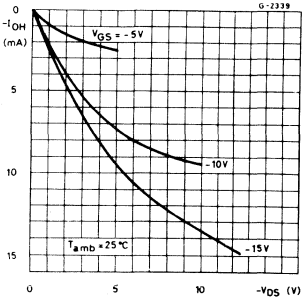


Fig. 5 - Typical propagation delay time vs. load capacitance (for 4054B)

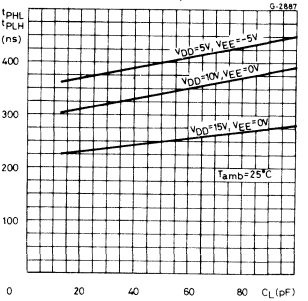


Fig. 6 - Typical propagation delay time vs. load capacitance for 4055B and 4056B)

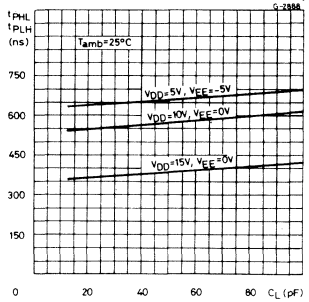


Fig. 7 - Typical transition time vs. load capacitance

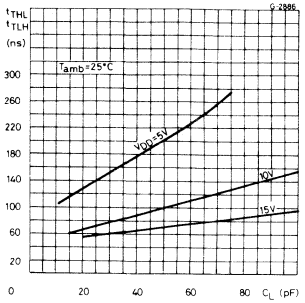
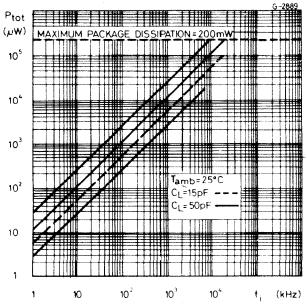


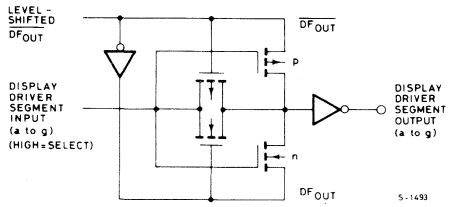
Fig. 8 - Typical dynamic power dissipation vs. frequency



TYPICAL APPLICATIONS

Fig. 9 - Display-driver circuit for one segment line and waveforms

(a)



(b)

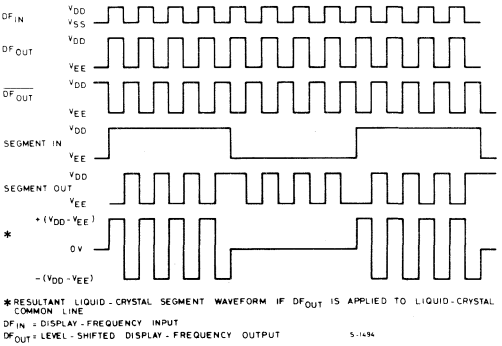


Fig. 10 - Clock display

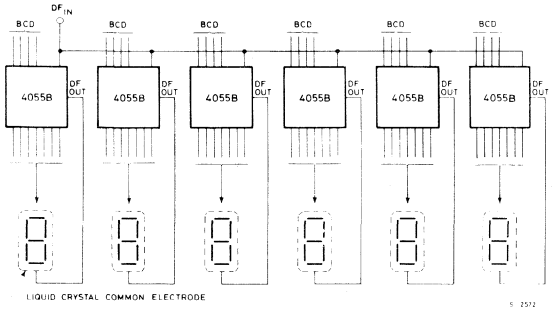
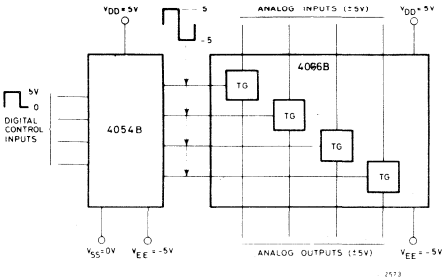


Fig. 11 - Digital (0 to +5V) to bidirectional analog control (+5 to -5V) level shifter



V_{DD}= 0V, V_{SS}= -5V, V_{EE}= -15V DF_{IN}= 30 Hz square wave.

TYPICAL APPLICATIONS (continued)

Fig. 12 - Single-digit liquid crystal display

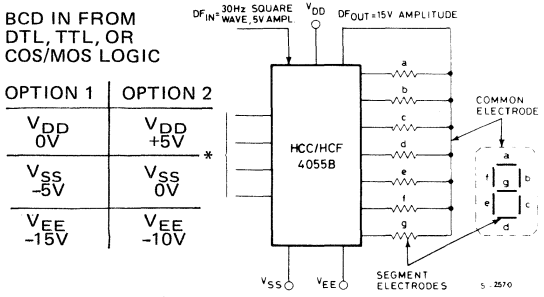


Fig. 13 - Conversion of "H" display to "F" display

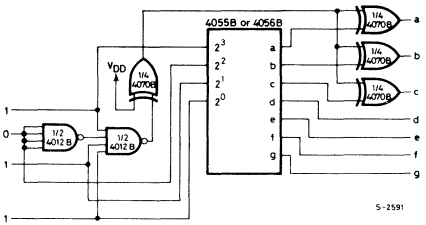
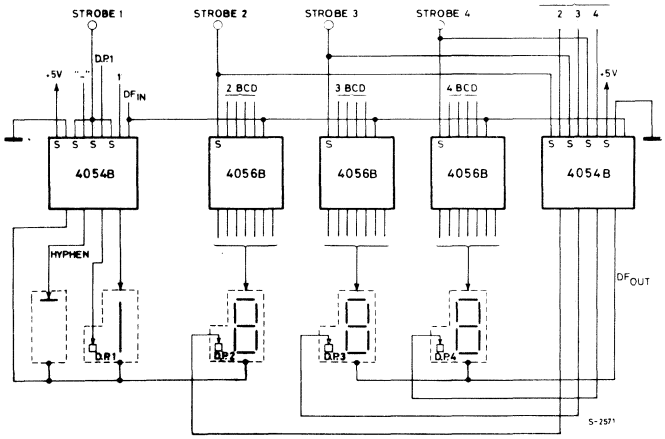


Fig. 14 - Typical 3½-digit liquid-crystal display: (V_{DD}=+5V, V_{SS}=0V, V_{EE}=-10V, DF_N=30Hz square wave)



In addition to the letters L, H, P, and A, five other letters can be displayed through the use of simple logic circuits preceding and following the **HCC/HCF 4055B** or **HCC/HCF 4056B** devices. Fig. 13 is an example of a circuit that converts an "H" display, (code 1011) to an "F" display. One condition that must be met is that $V_{EE} = V_{SS}$. If $V_{EE} \neq V_{SS}$, the **HCC/HCF 4054B** must be used to level shift in the appropriate places. In a similar manner the letters C, E, J,and U can be displayed.These circuits can also be used to drive LED displays provided the exclusive-OR gates have sufficient output-current drive. The letters B, D, G, I, O, and S may be represented by the codes for numbers 8, 0, 6, 1, 0, and 5, respectively, when there is preknowledge that only letters are to be displayed.

COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

14-STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDER AND OSCILLATOR

- MEDIUM-SPEED OPERATION
- COMMON RESET
- FULLY STATIC OPERATION
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4060B** (extended temperature range) and **HCF 4060B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4060B** consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of ϕ_1 (and ϕ_0). All inputs and outputs are fully buffered. Schmitt trigger action on the clock line permits unlimited clock rise and fall times.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

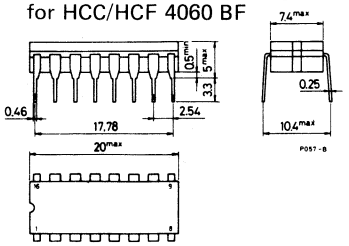
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

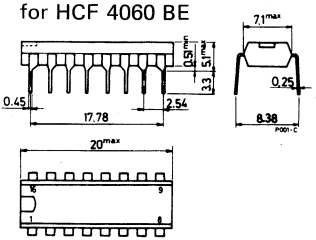
HCC 4060 BD for dual in-line ceramic package
HCC 4060 BF for dual in-line ceramic package, frit seal
HCC 4060 BK for ceramic flat package
HCF 4060 BE for dual in-line plastic package
HCF 4060 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

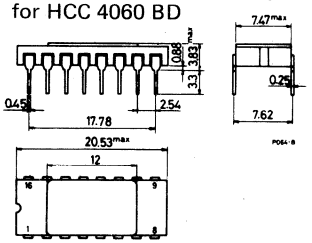
Dual in-line ceramic package for HCC/HCF 4060 BF



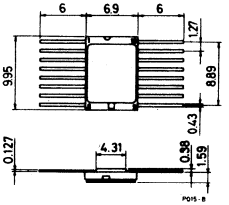
Dual in-line plastic package for HCF 4060 BE



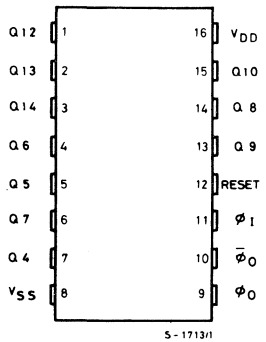
Dual in-line ceramic package for HCC 4060 BD



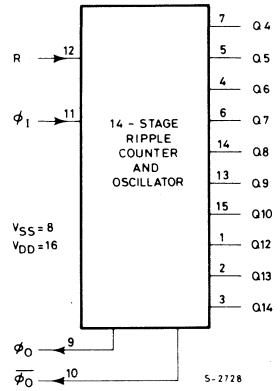
Ceramic flat package for HCC 4060 BK



CONNECTION DIAGRAM



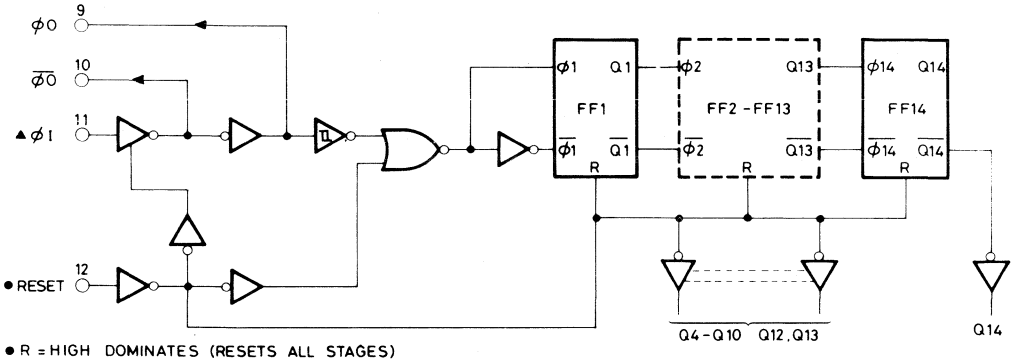
FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

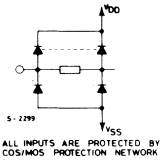
LOGIC DIAGRAM



● R = HIGH DOMINATES (RESETS ALL STAGES)

▲ COUNTER ADVANCES ONE BINARY COUNT ON EACH NEGATIVE-GOING TRANSITION OF φI (AND φO)

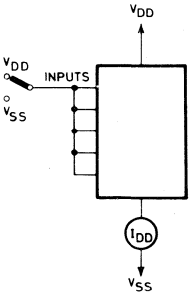
S-2729



ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

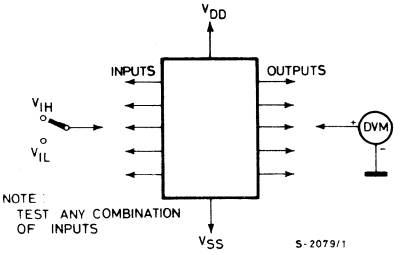
TEST CIRCUITS

Quiescent device current



S-1992/1

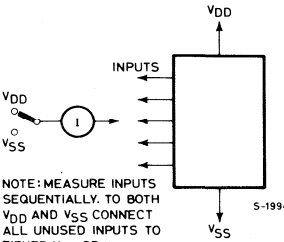
Input voltage



NOTE: TEST ANY COMBINATION OF INPUTS

S-2079/1

Input leakage current



NOTE: MEASURE INPUTS SEQUENTIALLY. TO BOTH V_{DD} AND V_{SS} CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}

S-1994/1

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

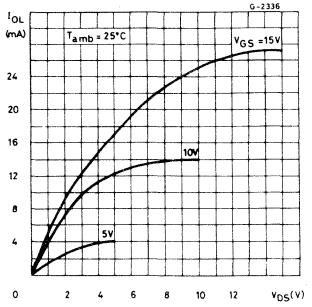
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

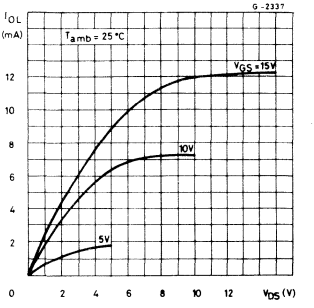
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions		Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
INPUT-PULSE OPERATION							
t_{PLH}, t_{PHL}	Propagation delay time (ϕ 1 to Q4 Out)		5		800		ns
			10		340		
			15		240		
t_{PLH}, t_{PHL}	Propagation delay time (Qn to Q_{n+1})		5		200		ns
			10		85		
			15		60		
t_{TLH}, t_{THL}	Transition time		5		100		ns
			10		50		
			15		40		
t_W	Input pulse width	f = 100 kHz	5		70		ns
			10		30		
			15		20		
t_r, t_f	Input pulse rise and fall time		5		Unlimited		μs
			10				
			15				
f_{max}	Maximum clock input frequency		5		7		MHz
			10		16		
			15		24		
RESET OPERATION							
t_{PHL}	Propagation delay time		5		300		ns
			10		140		
			15		100		
t_W	Reset pulse width		5		375		ns
			10		200		
			15		150		

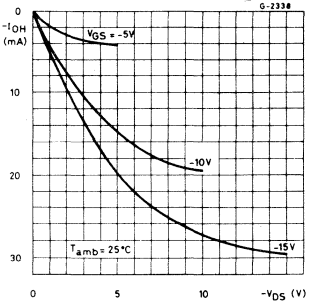
Minimum output low (sink) current characteristics



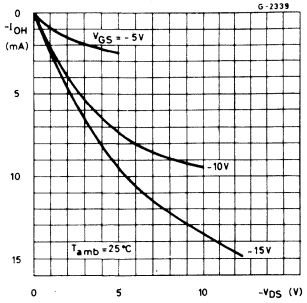
Typical output low (sink) current



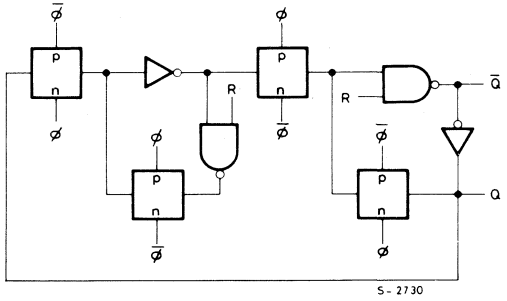
Minimum output high (source) current characteristics



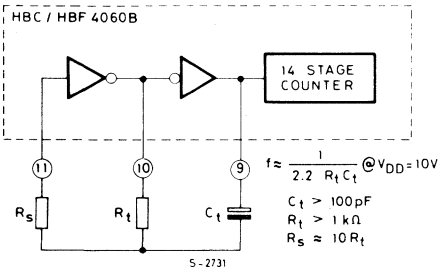
Typical output high (source) current characteristics



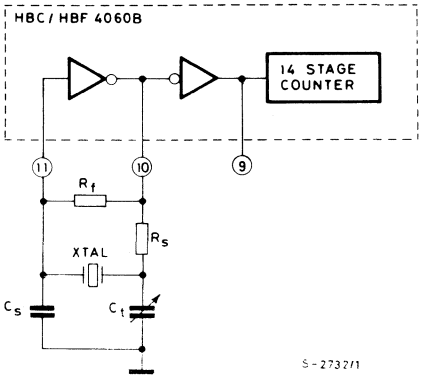
Detail of tipical flip-flop stage



Typical RC oscillator circuit



Typical crystal oscillator circuit



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

4-BIT MAGNITUDE COMPARATOR

- QUIESCENT CURRENT SPECIFIED TO 20V
- MAX. INPUT LEAKAGE CURRENT 1 μA @ 18V (FULL PACKAGE - TEMP. RANGE)
- STANDARD B-SERIES OUTPUT DRIVE
- EXPANSION to 8-16 ..... 4N BITS by CASCADING UNITS
- MEDIUM SPEED OPERATION: COMPARES TWO 4-BIT WORDS in 250 ns (TYP.) at 10V

The **HCC 4063B** (extended temperature range) and **HCF 4063B** (intermediate temperature range) are available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package.
The **HCC/HCF 4063B** is a low-power 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to" or "greater than" a second 4-bit word.
The **HCC/HCF 4063B** has eight comparing inputs (A3, B3, through A0, B0), three outputs ($A < B$, $A = B$, $A > B$) and three cascading inputs ($A < B$, $A = B$, $A > B$) that permit systems designers to expand the comparator function to 8, 12, 16 . . . . 4N bits. When a single **HCC/HCF 4063B** is used, the cascading inputs are connected as follows: ($A < B$) = low, ($A = B$) = high, ($A > B$) = low.
For words longer than 4 bits, **HCC/HCF 4063B** devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs ($A < B$, $A = B$, and $A > B$) on the least significant comparator are connected to a low, a high, and a low level, respectively.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

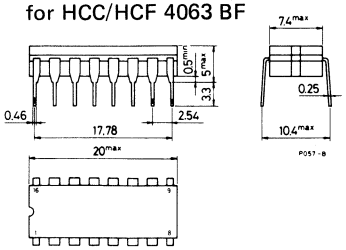
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

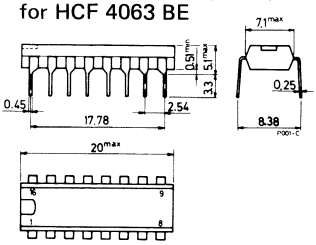
HCC 4063 BD for dual in-line ceramic package
HCC 4063 BF for dual in-line ceramic package, frit seal
HCC 4063 BK for ceramic flat package
HCF 4063 BE for dual in-line plastic package
HCF 4063 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

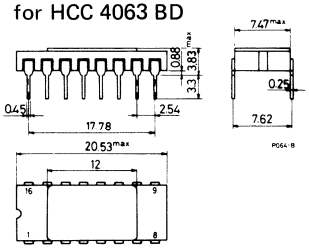
Dual in-line ceramic package
for HCC/HCF 4063 BF



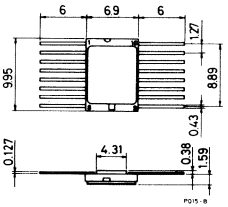
Dual in-line plastic package
for HCF 4063 BE



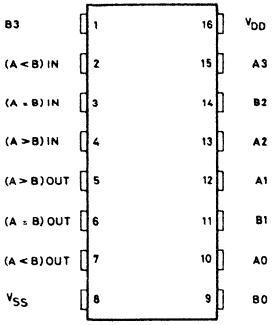
Dual in-line ceramic package
for HCC 4063 BD



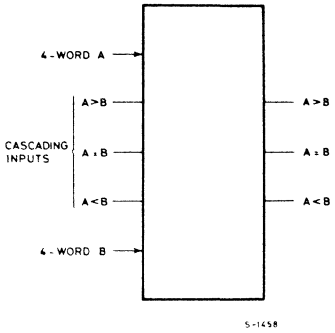
Ceramic flat package
for HCC 4063 BK



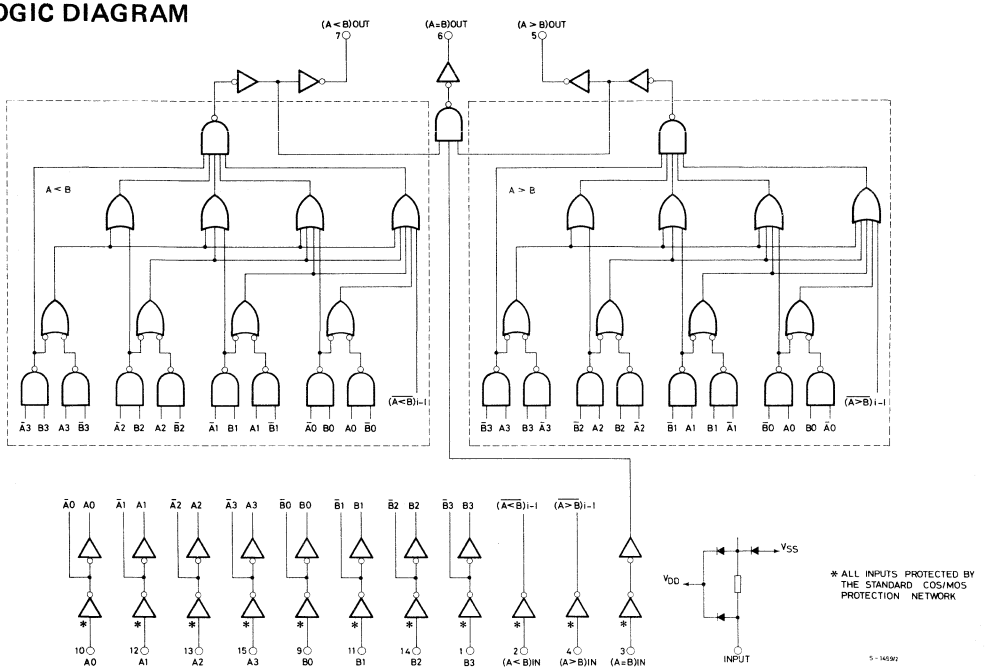
CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	X	0	0	1
A3=B3	A2>B2	X	X	X	X	X	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	X	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

X= Don't care
1 ≡ High state
0 ≡ Low state

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

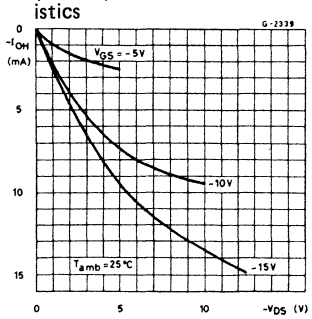
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

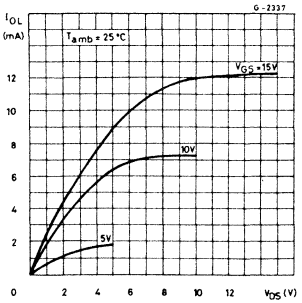
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	V_{DD} (V)	Values Min.	Typ.	Max.	Unit
t_{PLH}, t_{PHL} Propagation delay time	Comparing inputs to outputs	5		625	1250	ns
		10		250	500	
		15		175	350	
	Cascading inputs to outputs	5		500	1000	
		10		200	400	
		15		140	280	
t_{TLH} Transition time t_{THL}		5		100	200	ns
		10		50	100	
		15		40	80	

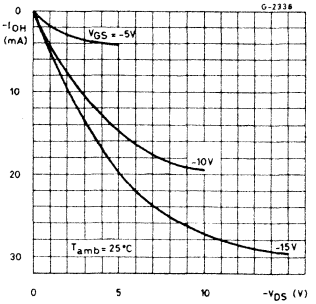
Minimum output high (source) current characteristics



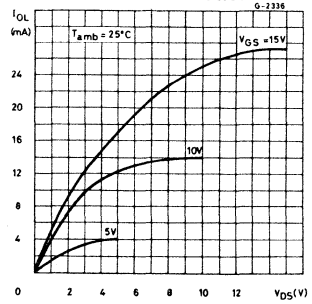
Minimum output low (sink) current characteristics



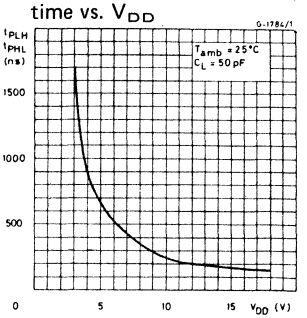
Typical output high (source) current characteristics



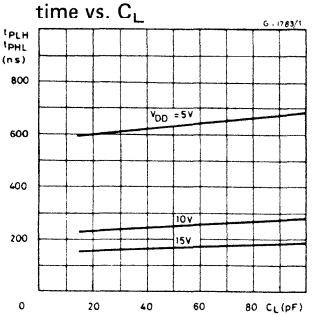
Typical output low (sink) current characteristics



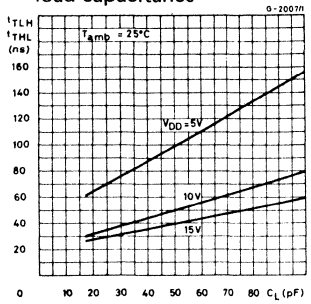
Typical propagation delay time vs. V_{DD}



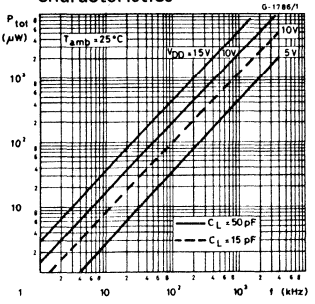
Typical propagation delay time vs. C_L



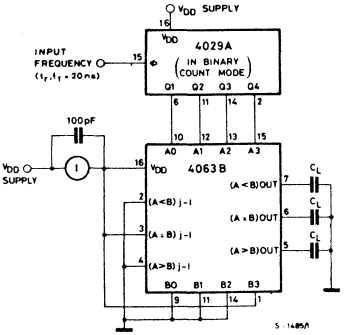
Typical transition time vs. load capacitance



Typical power dissipation characteristics

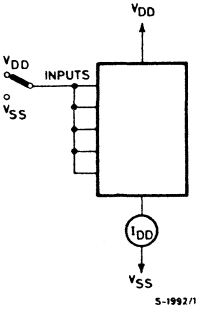


Dynamic power dissipation

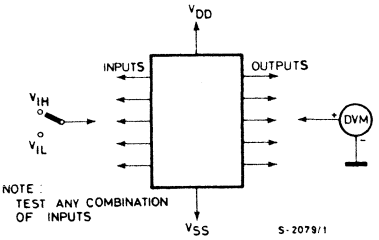


TEST CIRCUITS

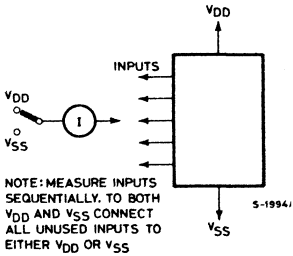
Quiescent device current



Noise immunity

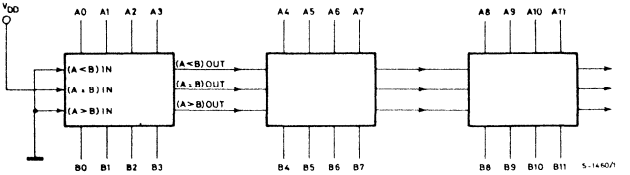


Input leakage current



TYPICAL APPLICATION

Typical speed characteristics of a 12-bit comparator



$t_{p\ (TOT.)} = t_p\ (^{COMPARE}_{INPUTS}) + 2 \times t_p\ (^{CASCADE}_{INPUTS})$ at $C_L = 50$ pF (each output), $V_{DD} = 10$V (3 stages)

$= 250 + 2 \times (200) = 650$ ns (typ.)

COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

QUAD BILATERAL SWITCH FOR TRANSMISSION OR MULTIPLEXING OF ANALOG OR DIGITAL SIGNALS

- 15V DIGITAL OR ± 7.5V PEAK-TO-PEAK SWITCHING
- 80Ω TYPICAL ON RESISTANCE FOR 15V OPERATION
- SWITCH ON RESISTANCE MATCHED TO WITHIN 5Ω OVER 15V SIGNAL-INPUT RANGE
- ON RESISTANCE FLAT OVER FULL PEAK-TO-PEAK SIGNAL RANGE
- HIGH ON/OFF OUTPUT-VOLTAGE RATIO: 65 dB TYP. @ f_{is}= 10 kHz, R_L= 10 kΩ
- HIGH DEGREE OF LINEARITY: < 0.5% DISTORTION TYP. @ f_{is} = 1 kHz, V_{is} = 5Vp-p, V_{DD}-V_{SS} ⩾ 10V, R_L= 10 kΩ
- EXTREMELY LOW OFF SWITCH LEAKAGE RESULTING IN VERY LOW OFFSET CURRENT AND HIGH EFFECTIVE OFF RESISTANCE; 10 pA TYP. @ V_{DD}-V_{SS}= 10V, T_A= 25°C
- EXTREMELY HIGH CONTROL INPUT IMPEDANCE (CONTROL CIRCUIT ISOLATED FROM SIGNAL CIRCUIT): 10^{12} Ω TYP.
- LOW CROSSTALK BETWEEN SWITCHES: -50 dB TYP. @ f_{is}= 0.9 MHz, R_L= 1 kΩ
- MATCHED CONTROL-INPUT TO SIGNAL-OUTPUT CAPACITANCE: REDUCES OUTPUT SIGNAL TRANSIENTS
- FREQUENCY RESPONSE, SWITCH ON = 40 MHz (TYP.)
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4066B** (extended temperature range) and **HCF 4066B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4066B** is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with **HCC/HCF 4016B**, but exhibits a much lower ON resistance. In addition, the ON resistance is relatively constant over the full input-signal range, The **HCC/HCF 4066B** consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased ON or OFF simultaneously by the control signal. As shown in schematic diagram, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range. The advantages over single-channel switches include peak input signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range. For sample-and-hold applications, however, the **HCC/HCF 4016B** is recommended.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

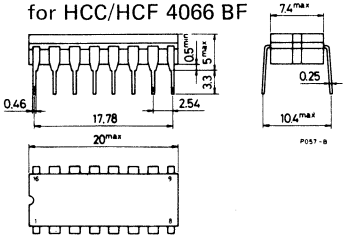
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

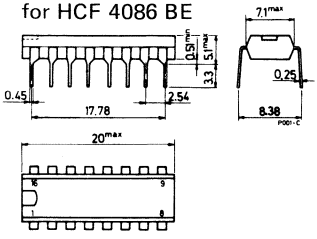
HCC 4066 BD for dual in-line ceramic package
HCC 4066 BF for dual in-line ceramic package, frit seal
HCC 4066 BK for ceramic flat package
HCF 4066 BE for dual in-line plastic package
HCF 4066 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

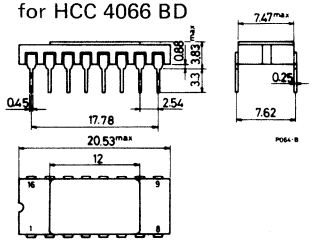
Dual in-line ceramic package
for HCC/HCF 4066 BF



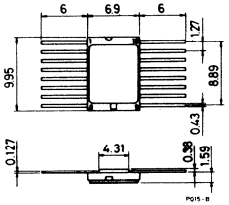
Dual in-line plastic package
for HCF 4086 BE



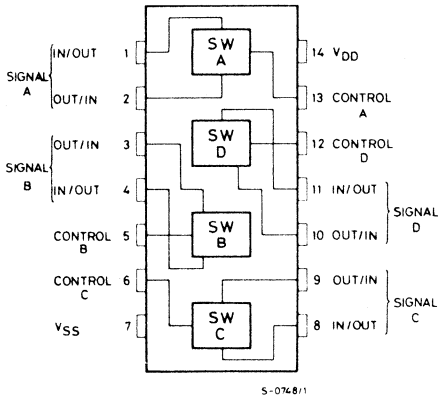
Dual in-line ceramic package
for HCC 4066 BD



Ceramic flat package
for HCC 4066 BK



FUNCTIONAL DIAGRAM

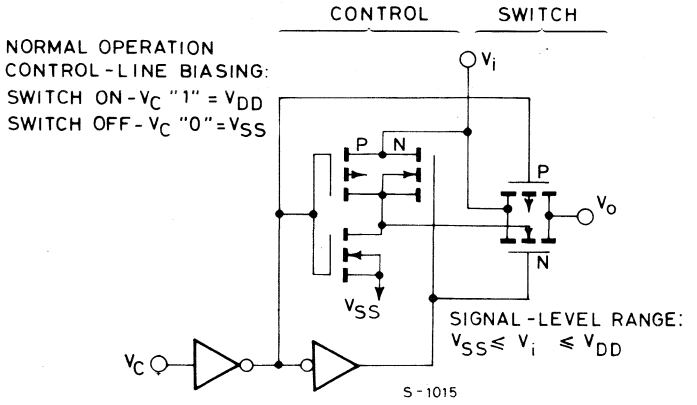


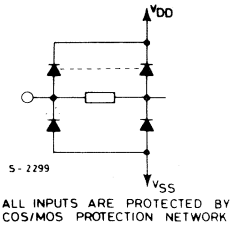
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

SCHEMATIC DIAGRAM

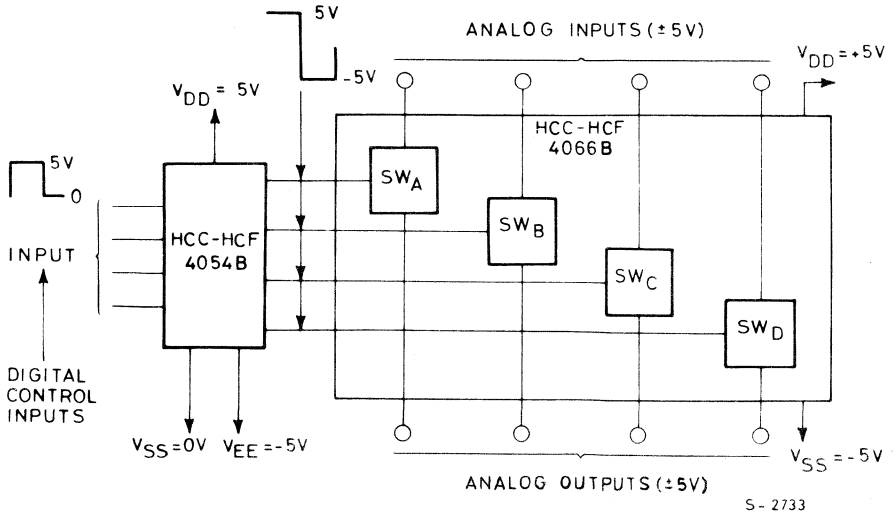
1 of 4 identical switches and its associated control circuitry





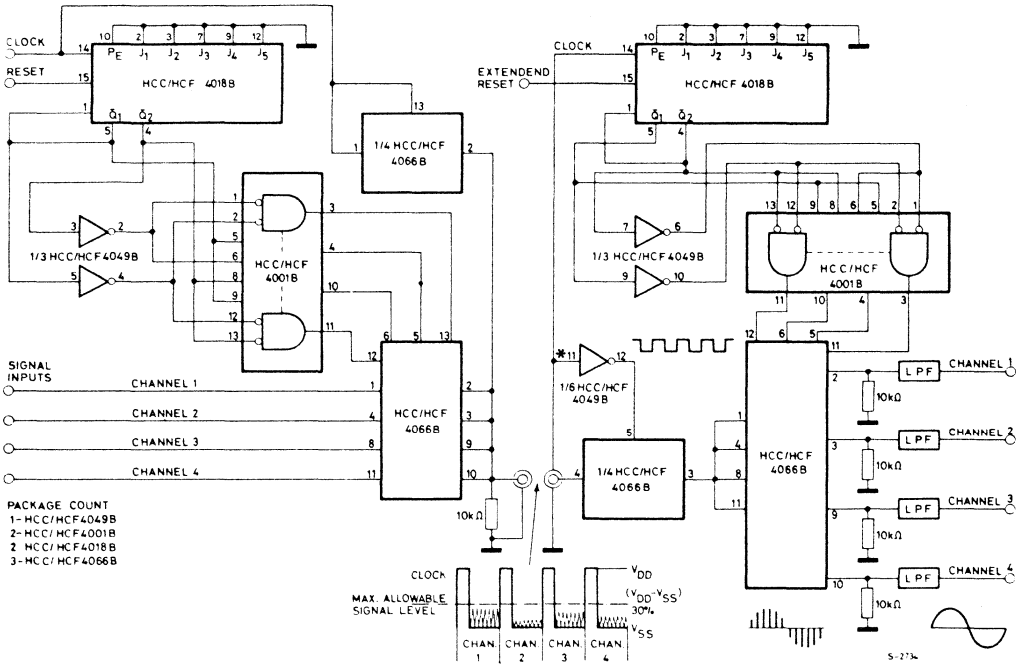
TYPICAL APPLICATIONS

Bidirectional signal transmission via digital control logic



TYPICAL APPLICATIONS (continued)

4-channel PAM multiplex system diagram



ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions							Typ.	Unit
		R_L• (KΩ)	V_C= V_{DD}	V_{SS} (V)	V_{IS} (V)	V_{DD} (V)	f_i (KHz)			
I_{DD}	Quiescent device current (All switches ON or all switches OFF)					5			0.01	μA
						10			0.01	
						15			0.01	
						20			0.02	
Signal Inputs (V_{IS}) and Outputs (V_{OS})										
R_{ON}	ON Resistance	10	+7.5	-7.5	-7.5 to +7.5				80	Ω
		10	+15	0	0 to 15					
		10	+5	-5	-5 to +5				120	
		10	+10	0	0 to +10					
		10	+2.5	-2.5	-2.5 to +2.5				250	
		10	-5	0	0 to +5					
ΔON	Resistance Between Any 2 of 4 Switches ΔR_{ON}	10	+7.5	-7.5	+7.5 to -7.5				5	
			+15	0	+15 to 0					
		10	+5	-5	+5 to -5				10	
			+10	0	+10 to 0					
		10	+2.5	-2.5	-2.5 to +2.5				25	
			+5	0	0 to 5					
Sine wave response (Distortion)		10	+5	-5	5 pp▲		1		0.4	%
Frequency response switch ON (Sine wave input)		1	+5	-5	5 pp			$20 \log 10 \frac{V_{OS}}{V_{IS}} = -3$ dB	40	MHz
Feedthrough switch OFF		1	+5	-5		-5 pp		$20 \log 10 \frac{V_{OS}}{V_{IS}} = -50$ dB	1.25	MHz
Input or output leakage current switch OFF				-7.5		+7.5			± 0.1	nA
				-5		+5			± 0.1	
Crosstalk between any 2 of 4 switches (f = -50 dB)		1	+5(A)	-5 (B)	5 pp			$20 \log 10 \frac{V_{OS(B)}}{V_{IS(A)}} = -50$dB	0.9	MHz

• For all test conditions
Δ Symmetrical about 0V

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test conditions							Typ.	Unit
	R_L• (KΩ)	V_C= V_{DD}	V_{SS} (V)	V_{IS} (V)	V_{DD} (V)	f_i (KHz)			
Propagation delay			GND	10 Sq.Wave	5		C_L= 50 pF $t_r = t_f$ = 20 ns	40	ns
					10			20	
					15			15	
C_{IS} Input capacitance			-5		+5			8	pF
C_{OS} Output capacitance								8	
C_{IOS} Feedthrough								0.5	
CONTROL (V_C)									
V_{TH} Switch threshold voltage					5		I_{is}= 10 μA	2.25	V
					10			4.5	
					15			6.75	
I_{IN} Input current				⩽ V_{DD}	18		V_{DD}-V_{SS}= 18 V_{CC} ⩽ V_{DD}-V_{SS}	±10^{-5}	μA
Crostalk (control input to signal output)	10				10		V_C= 10 (Sq-wave) $t_r = t_f$= 20 ns	50	mW
Turn-on propagation delay	1				5		V_{DD}-V_{SS}= 10 $t_r = t_f$ = 20 ns C_L= 50 pF	35	ns
					10			20	
					15			15	
Maximum allowable control input repetition rate	1		GND		10		C_L= 50 pF V_C= 10 (Sq. Wave) $t_r = t_f$ = 20 ns	10	MHz
C_{IN} Input capacitance								5	pF

COS/MOS INTEGRATED CIRCUITS

HCC/HCF 4067B
HCC/HCF 4097B

PRELIMINARY DATA

ANALOG MULTIPLEXERS/DEMULTIPLEXERS:

4067B SINGLE 16-CHANNEL
4097B DIFFERENTIAL 8-CHANNEL

- LOW ON RESISTANCE: 125Ω (TYP.) OVER 15 Vp-p SIGNAL-INPUT RANGE FOR V_{DD}-V_{SS}= 15V
- HIGH OFF RESISTANCE: CHANNEL LEAKAGE OF ± 10 pA (TYP.) @V_{DD}-V_{SS}= 10V
- MATCHED SWITCH CHARACTERISTICS: ΔR_{ON}= 5Ω (TYP.) FOR V_{DD}-V_{SS}= 15V
- VERY LOW QUIESCENT POWER DISSIPATION UNDER ALL DIGITAL-CONTROL INPUT AND SUPPLY CONDITIONS: 0.2 μW (TYP.) @V_{DD}-V_{SS}= 10V
- BINARY ADDRESS DECODING ON CHIP
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4067B, HCC 4097B** (extended temperature range) and **HCF 4067B, HCF 4097B**(intermediate temperature range) are monolithic-integrated circuit, available in 24-lead dual in-line plastic and ceramic slam package.
The **HCC/HCF 4067** and **HCC/HCF 4097** COS/MOS analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.
The **HCC/HCF 4067** is a 16-channel multiplexer with four binary control inputs, A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.
The **HCC/HCF 4097** is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches. A logic "1" present at the inhibit input turns all channels off.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

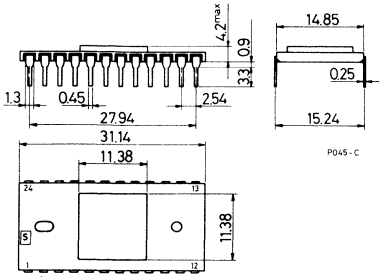
ORDERING NUMBERS:

HCC 4XXX BD for dual in-line ceramic slam package
HCF 4XXX BD for dual in-line ceramic slam package
HCF 4XXX BE for dual in-line plastic package

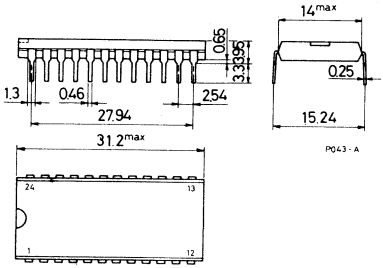
HCC/HCF 4067B
HCC/HCF 4097B

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic slam package
for HCC/HCF 4XXX BD

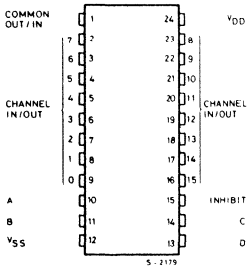


Dual in-line plastic package
for HCF 4XXX BE

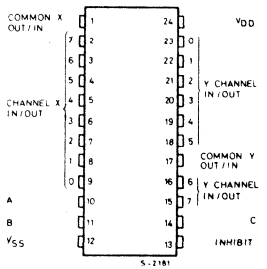


CONNECTION DIAGRAMS

For **HCC/HCF 4067B**

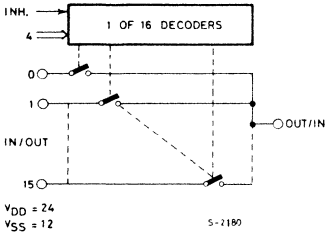


For **HCC/HCF 4097B**

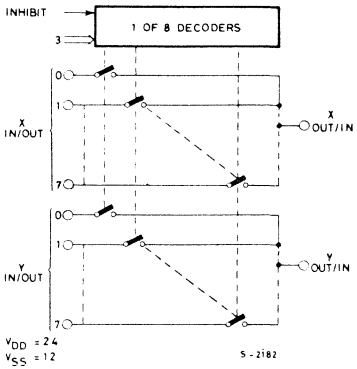


FUNCTIONAL DIAGRAMS

For **HCC/HCF 4067B**

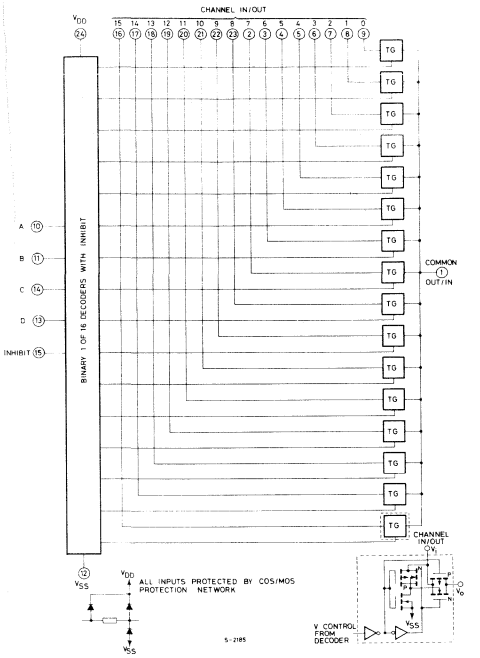


For **HCC/HCF 4097B**

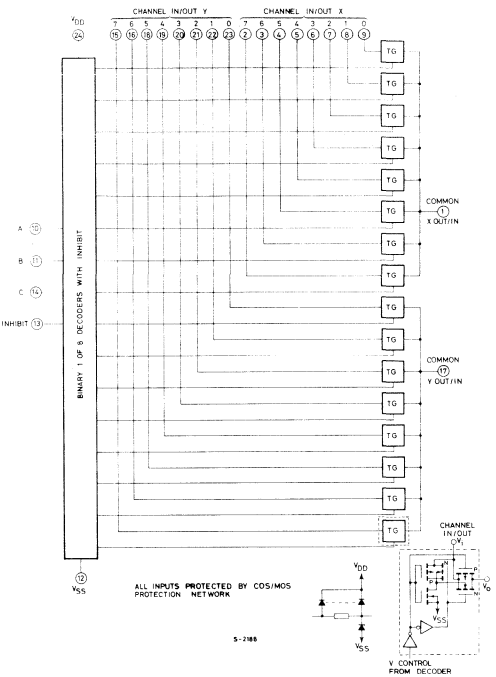


LOGIC DIAGRAMS

For HCC/HCF 4067B



For HCC/HCF 4097B



TRUTH TABLES

For HCC/HCF 4067B

A	B	C	D	Inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

For HCC/HCF 4097B

A	B	C	Inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions V_I (V)	V_{SS} (V)	V_{DD} (V)	Values T_{Low} (*) Min.	T_{Low} (*) Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High} (*) Min.	T_{High} (*) Max.	Unit
I_L	Quiescent device current				5		5		0.04	5		150	μA
					10		10		0.04	10		300	
					15		20		0.04	20		600	
					20		100		0.08	100		3000	
SWITCH													
ON	Resistance	HCC	$V_{SS} \leqslant V_I \leqslant V_{DD}$	0	5		2000		470	2500		3500	Ω
					10		310		180	400		580	
					15		220		125	280		400	
		HCF	$V_{SS} \leqslant V_I \leqslant V_{DD}$	0	5		2100		470	2500		3200	
					10		330		180	400		520	
					15		230		125	280		360	
ΔON	Resistance ΔR_{ON} (Between any 2 channels)			0	5				10				Ω
					10				10				
					15				5				
OFF	Channel (•) Leakage current	Any channel OFF	$V_{SS} \leqslant V_I \leqslant V_{DD}$	0	10		± 200		± 0.1	± 200		± 200	nA
					15		± 500		± 0.1	± 200		± 500	
					20		±1000		± 0.1	± 200		±1000	
		All channels OFF (common OUT/IN)	$V_{SS} \leqslant V_I \leqslant V_{DD}$	0	10		± 200		± 0.1	± 200		± 200	nA
					15		± 500		± 0.1	± 200		± 500	
					20		±1000		± 0.1	± 200		±1000	
C	Capacitance	Input		-5	5				5				pF
		Output 4067B		-5	5				55				
		Output 4097B		-5	5				35				
		Feed-through		-5	5				0.2				
CONTROL (Address or Inhibit)													
V_{IL}	Input low voltage		R_L = 1 kΩ . (connected to V_{SS}) I_I < 2 μA (on all OFF channels) V_I=V_{DD} thru 1 kΩ	0	5		1.5			1.5		1.5	V
					10		3			3		3	
					15		4			4		4	
V_{IH}	Input high voltage			0	5	3.5		3.5			3.5		V
					10	7		7			7		
					15	11		11			11		
I_{IH},I_{IL}	Input leakage current		V_I= 0/18V	0	18		± 0.1		± 10^{-5}	± 0.1		± 1	μA
C_i	Input capacitance		Any address or inhibit input						5	7.5			pF

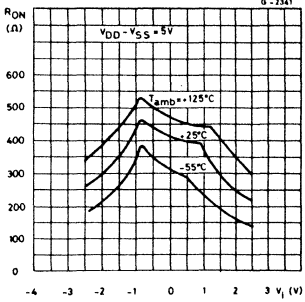
(•) Determined by minimum feasible leakage measurement for automatic testing
(*) T_{LOW}= -55°C for HCC device; -40°C for HCF device.
T_{High}= +125°C for HCC device; +85°C for HCF device.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF all input square wave rise and fall times = 20 ns)

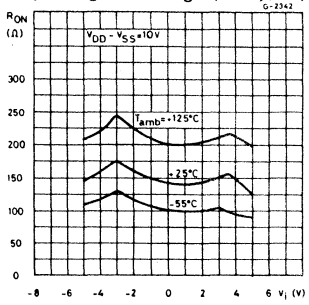
Parameter	Test conditions								Values		Unit
	V_C (V)	R_L (kΩ)	f_i (KHz)	V_I (V)	V_{SS} (V)	V_{DD} (V)			Typ.	Max.	
SWITCH											
t_{pd} Propagation delay time (Signal Input to output)	= V_{DD}	10		V_{DD} 0	0	5			30		ns
						10			15		
						15			11		
Frequency Response Channel "ON" (Sine Wave Input) at 20 Log $\frac{V_o}{V_I}$ = -3dB	= V_{DD}	1		5(•)	0	10	V_o at Common OUT/IN	4067B	14		MHz
								4097B	20		
							V_o at Any Channel		60		
Feedthrough (All channels OFF) at 20 Log $\frac{V_o}{V_I}$ = -40 dB	= V_{SS}	1		5(•)	0	10	V_o at Common OUT/IN	4067B	20		MHz
								4097B	12		
							V_o at Any channel		8		
Frequency Signal Crosstalk at 20 Log $\frac{V_o(B)}{V_I(A)}$ = -40dB	$V_{C(A)}=V_{DD}$ $V_{C(B)}=V_{SS}$	1		5(•)	0	10	Between Any 2 (A and B) channels		1		MHz
							Between sections (A and B) 4097B only	Measured on common	10		
								Measured on Any channel	18		
Sine wave Distortion	5	10	1	2(•)	0	5			0.3		%
	10	10	1	3(•)	0	10			0.2		
	15	10	1	5(•)	0	15			0.12		
CONTROL (Address or Inhibit)											
Propagation delay time: Address or Inhibit to signal OUT (channel turning ON)	V_{DD} 0	10			0	5			325	650	ns
					0	10			135	270	
					0	15			95	190	
Propagation delay time: Address or Inhibit to signal OUT (channel turning OFF)	V_{DD} 0	0.3			0	5			220	440	ns
					0	10			90	180	
					0	15			65	130	
Address or Inhibit to Signal Crosstalk	V_{DD} 0	10*			0	10			75		mV peak

(•) Peak to peak voltage symmetrical about $\frac{V_{DD} - V_{SS}}{2}$
(*) Both ends of channel

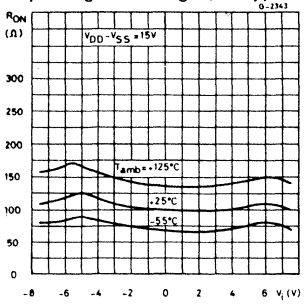
Typical ON resistance vs. input signal voltage (all types)



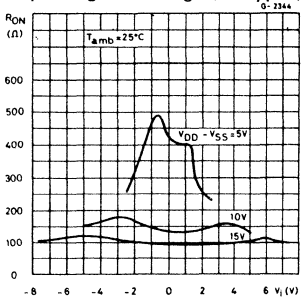
Typical ON resistance vs. input signal voltage (all types)



Typical ON resistance vs. input signal voltage (all types)



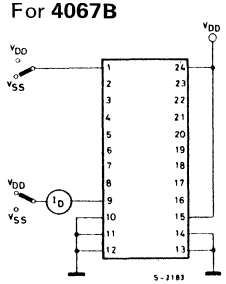
Typical ON resistance vs. input signal voltage (all types)



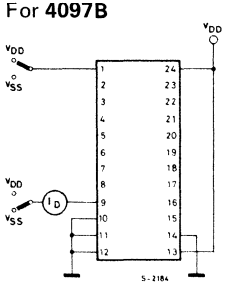
TEST CIRCUITS

OFF channel leakage current-any channel OFF

For **4067B**

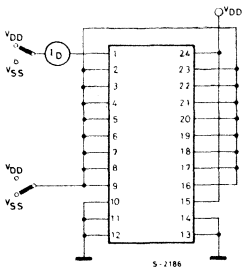


For **4097B**

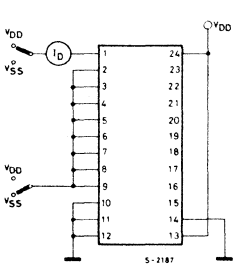


OFF channel leakage current-all channels OFF

For **4067B**



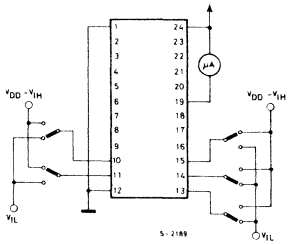
For **4097B**



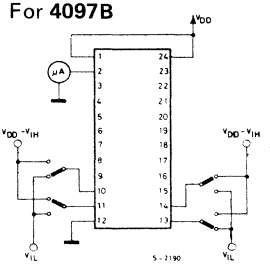
TEST CIRCUITS (continued)

Input voltage-measure $< 2\ \mu A$ on all OFF channels (e.g. channel 12)

For **4067B**

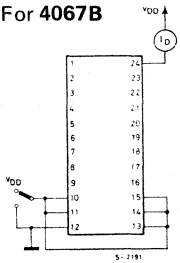


For **4097B**

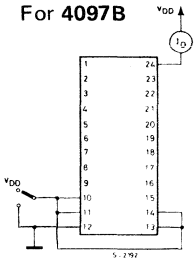


Quiescent device current

For **4067B**

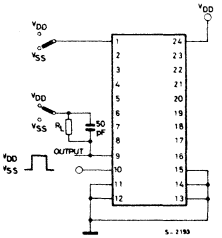


For **4097B**

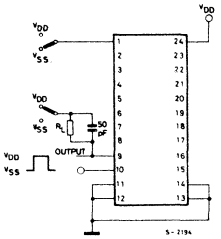


Turn-on and turn-off propagation delay-address select input to signal output (e.g. measured on channel 0)

For **4067B**

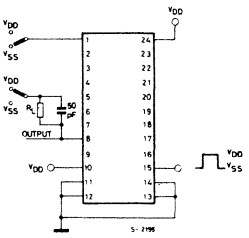


For **4097B**

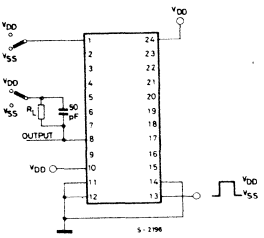


Turn-on and turn-off propagation delay-inhibit input to signal output (e.g. measured on channel 1)

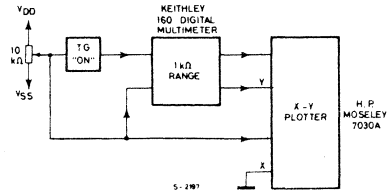
For **4067B**



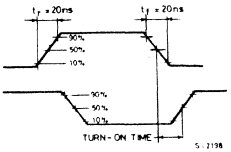
For **4097B**



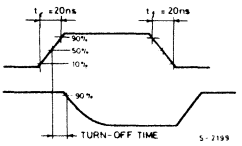
Channel ON resistance measurement circuit



Propagation delay waveform channel being turned ON ($R_L = 10\ k\Omega$, $C_L = 50$ pF)



Propagation delay waveform channel being turned OFF ($R_L = 300\Omega$, $C_L = 50$ pF)



APPLICATIONS INFORMATION

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L= effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the **HCC/HCF 4067B** or **HCC/HCF 4097B**.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned on or off by an address input, there is a momentary conductive path from the channel to V_{SS}, which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to V_{SS}.

The amount of charge dumped is mostly a function of the signal level above V_{SS}. Typically, at V_{DD}-V_{SS}= 10V, a 100 pF capacitor connected to the input or output of the channel will lose 3-4% of its voltage at the moment the channel turns on or off. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2 μs. When the inhibit signal turns a channel off, there is no charge dumping to V_{SS}. Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to capacitive coupling from inhibit input to channel input or output. Address inputs also couple some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the **HCC/HCF 4067B**, terminals 1 and 17 on the **HCC/HCF 4097B.**

COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

8 - INPUT NAND/AND GATE

- MEDIUM-SPEED OPERATION - t_{PHL}, t_{PLH} = 75 ns (TYP.) AT 10V
- BUFFERED OUTPUT
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT LEAKAGE CURRENT 1 μA AT 18V (FULL PACKAGE-TEMP. RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4068B** (extended temperature range) and **HCF 4068B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package, and ceramic flat package. The **HCC/HCF 4068B** NAND/AND gate provides the system designer with direct implementation of the positive-logic 8-input NAND and AND functions and supplements the existing family of COS/MOS gates.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

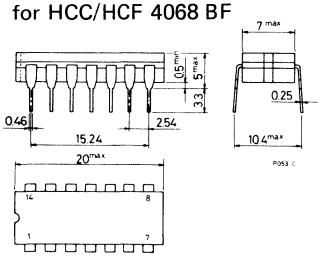
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

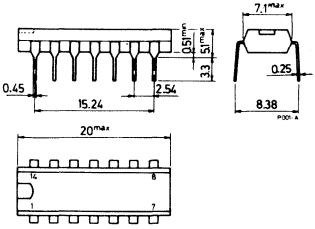
HCC 4068 BD for dual in-line ceramic package
HCC 4068 BF for dual in-line ceramic package,frit seal
HCC 4068 BK for ceramic flat package
HCF 4068 BE for dual in-line plastic package
HCF 4068 BF for dual in-line ceramic package,frit seal

MECHANICAL DATA (dimensions in mm)

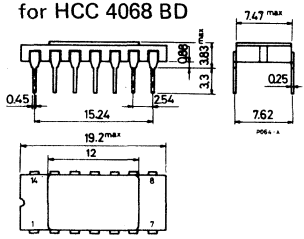
Dual in-line ceramic package
for HCC/HCF 4068 BF



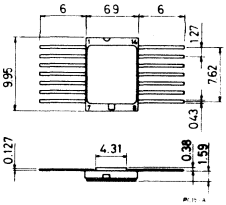
Dual in-line plastic package
for HCF 4068 BE



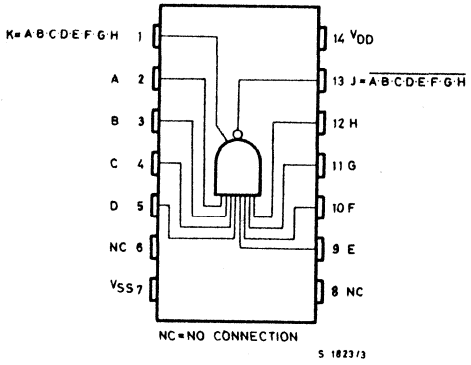
Dual in-line ceramic package
for HCC 4068 BD



Ceramic flat package
for HCC 4068 BK



CONNECTION DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

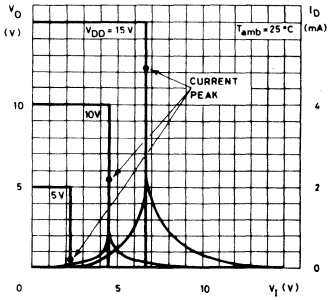
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				2/13	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13/2	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

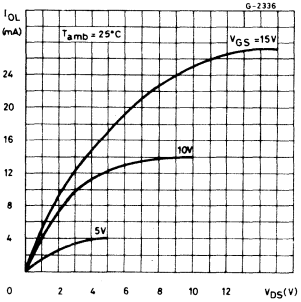
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 KΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH} Propagation delay time		5		150	300	ns
		10		75	150	
		15		55	110	
t_{TLH}, t_{THL} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	

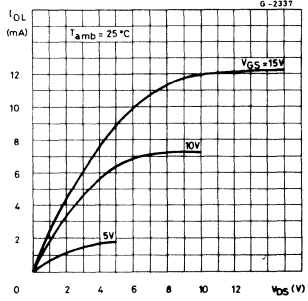
Typical voltage and current transfer characteristics



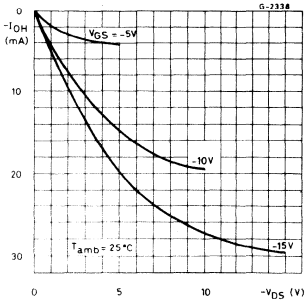
Typical output low (sink) current characteristics



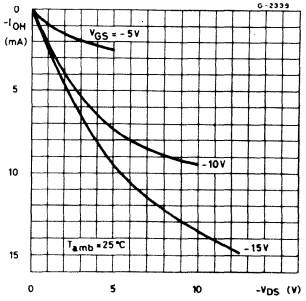
Minimum output low (sink) current characteristics



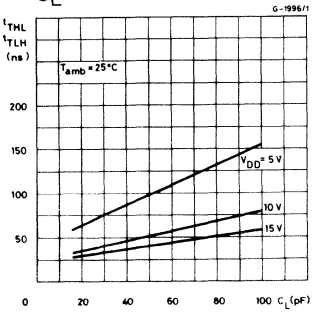
Typical output-p-channel drain characteristics



Minimum output-p-channel drain characteristics

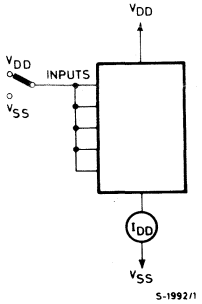


Typical transition time vs. C_L

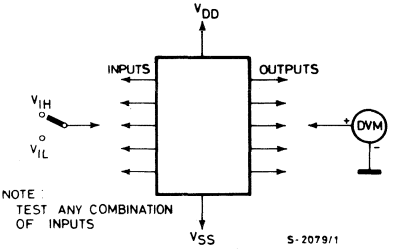


TEST CIRCUITS

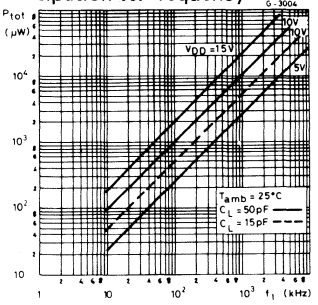
Quiescent device current



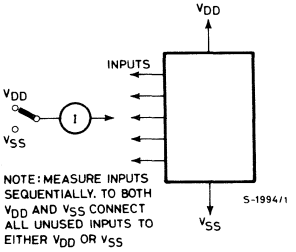
Input voltage



Typical dynamic power dissipation vs. frequency



Input current



COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

HEX INVERTER

- MEDIUM-SPEED OPERATION - t_{PHL}, t_{PLH}= 30 ns (TYP.) AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT LEAKAGE OF 1 μA AT 18V (FULL PACKAGE TEMPERATURE RANGE)
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4069 UB** (extended temperature range) and **HCF 4069 UB** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4069 UB** consists of six COS/MOS inverter circuits. This device is intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as **HCC/HCF 4049B** Hex Inverter/Buffers are not required.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature rang	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

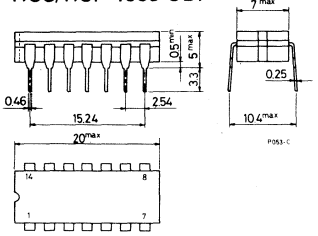
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

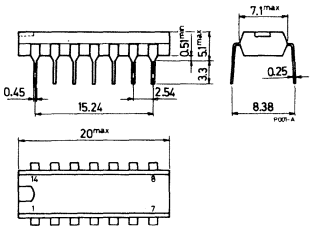
HCC 4069 UBD for dual in-line ceramic package
HCC 4069 UBF for dual in-line ceramic package, frit seal
HCC 4069 UBK for ceramic flat package
HCF 4069 UBE for dual in-line plastic package
HCF 4069 UBF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

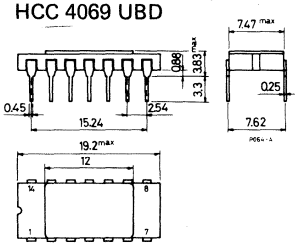
Dual in-line ceramic package for HCC/HCF 4069 UBF



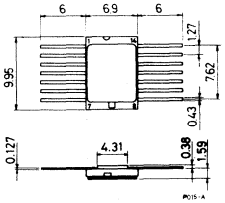
Dual in-line plastic package for HCF 4069 UBE



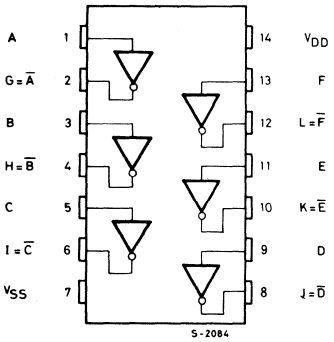
Dual in-line ceramic package for HCC 4069 UBD



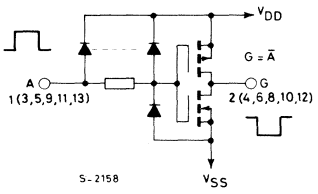
Ceramic flat package for HCC 4069 UBK



CONNECTION DIAGRAM



Schematic diagram of one of six identical inverters



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

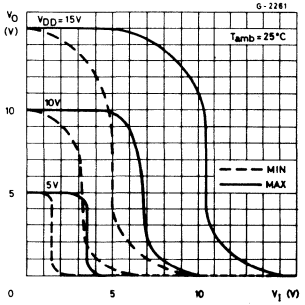
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	4		4			4		V
				1/9	< 1	10	8		8			8		
				2/13	< 1	15	12		12			12		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1			1		1	V
				9/1	< 1	10		2			2		2	
				13/2	< 1	15		3			3		3	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}	Input leakage current		0/18	Any input		18		$\pm$0.1		$\pm 10^{-5}$	$\pm$0.1		$\pm$1	μA
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

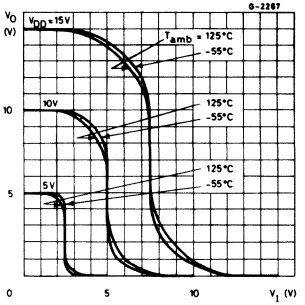
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD}= 0.3%/°C values, all input rise and fall time = 20 ns)

Parameter	Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time		5		55	110	ns
		10		30	60	
		15		25	50	
t_{TLH}, t_{THL} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	

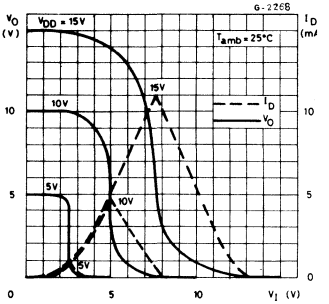
Minimum and maximum voltage transfer characteristics



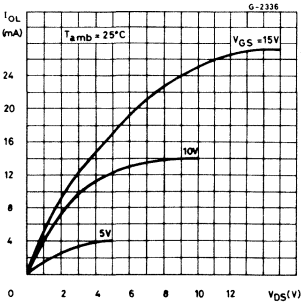
Typical voltage transfer characteristics as a function of temperature



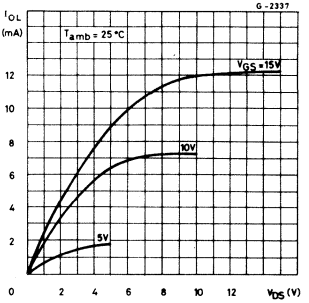
Typical current and voltage transfer characteristics



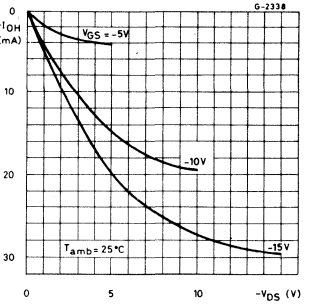
Typical output low (sink) current characteristics



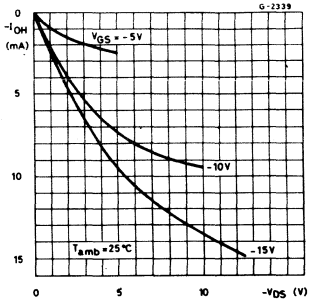
Minimum output low (sink) current characteristics



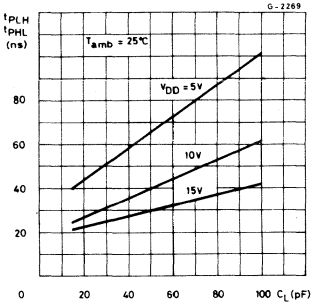
Typical output high (source) current characteristics



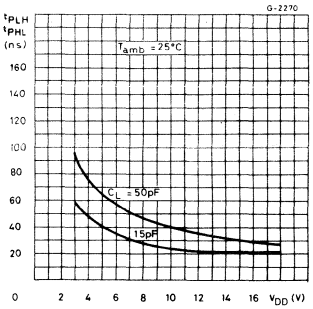
Minimum output high (source) current characteristics



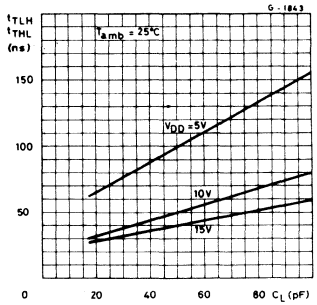
Typical propagation delay time vs. load capacitance



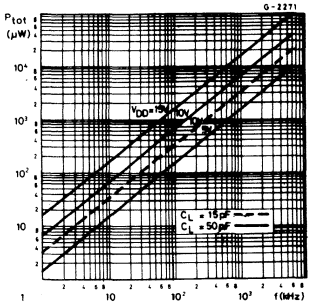
Typical propagation delay time vs. supply voltage



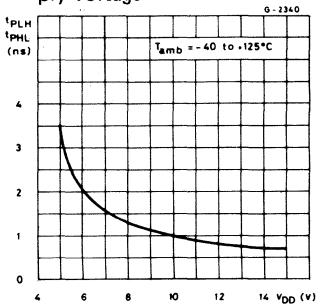
Typical transition time vs. load capacitance



Typical dynamic power dissipation/per inverter vs. frequency

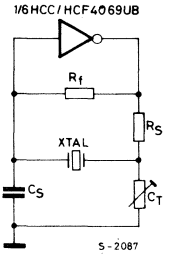


Variation of normalized propagation delay time (t_{PHL} and t_{PLH}) with supply voltage

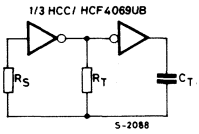


APPLICATIONS

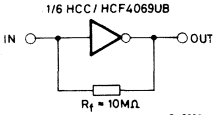
Typical crystal oscillator circuit



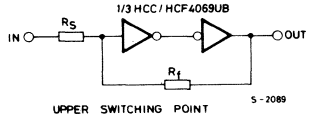
Typical RC oscillator circuit



High-input impedance amplifier



Input pulse shaping circuit (Schmitt trigger)



UPPER SWITCHING POINT

$$V_P = \frac{R_S \cdot R_f}{R_f} \cdot \frac{V_{DD}}{2}$$

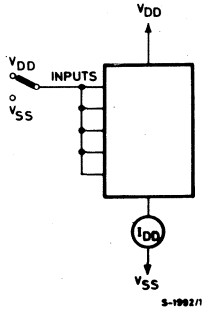
LOWER SWITCHING POINT

$$V_N = \frac{R_f - R_S}{R_f} \cdot \frac{V_{DD}}{2}$$

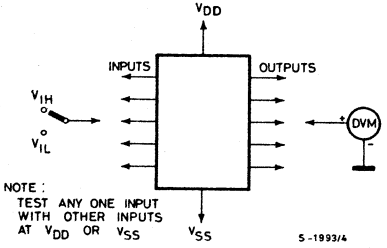
$R_f > R_S$

TEST CIRCUITS

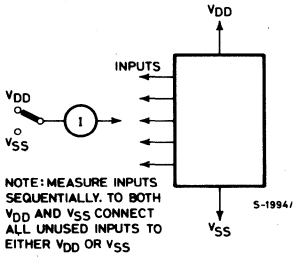
Quiescent device current



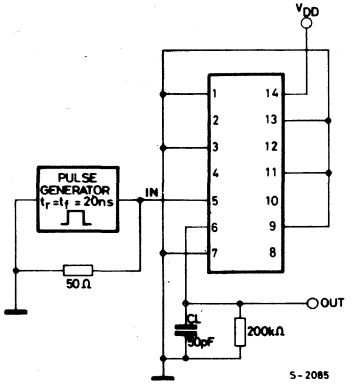
Noise immunity

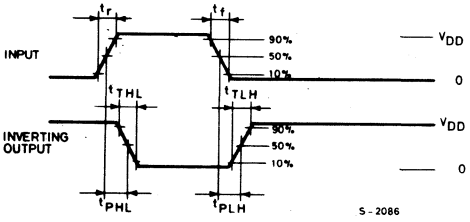


Input leakage current



Dynamic electrical characteristics and waveforms





COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

4070B - QUAD EXCLUSIVE-OR GATE
4077B - QUAD EXCLUSIVE-NOR GATE

- MEDIUM-SPEED OPERATION $t_{PHL}= t_{PLH}= 70$ ns (TYP.) at $V_{CC}= 10V$, $C_L= 50$ pF
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT LEAKAGE OF 1 μA at 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V AND 15V PARAMETRIC RATING

The **HCC 4070B/4077B** (extended temperature range) and **HCF 4070B/4077B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4070B** contains four independent exclusive-OR gates.
The **HCC/HCF 4077B** contains four independent exclusive-NOR gates.
The **HCC/HCF 4070B** and **HCC/HCF 4077B** provide the system designer with a means for direct implementation of the exclusive-OR and exclusive-NOR function, respectively. For applications as Logical comparators, Adders/subtractors, Parity generators and checkers.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

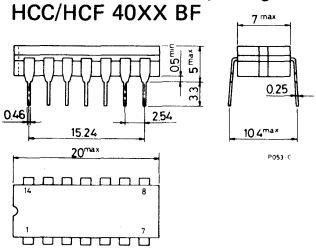
ORDERING NUMBERS:

HCC 40XX BD for dual in-line ceramic package
HCC 40XX BF for dual in-line ceramic package, frit seal
HCC 40XX BK for ceramic flat package
HCF 40XX BE for dual in-line plastic package
HCF 40XX BF for dual in-line ceramic package, frit seal

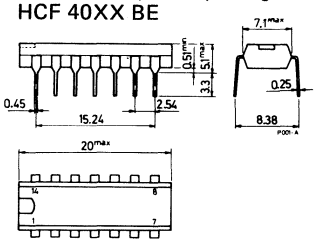
HCC/HCF 4070 B
HCC/HCF 4077 B

MECHANICAL DATA (dimensions in mm)

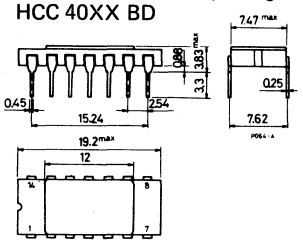
Dual in-line ceramic package for HCC/HCF 40XX BF



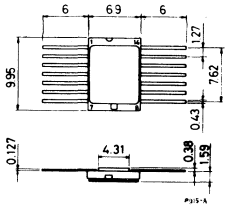
Dual in-line plastic package for HCF 40XX BE



Dual in-line ceramic package for HCC 40XX BD

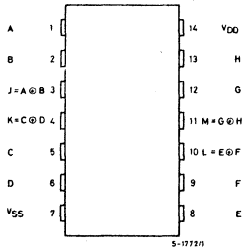


Ceramic flat package for HCC 40XX BK

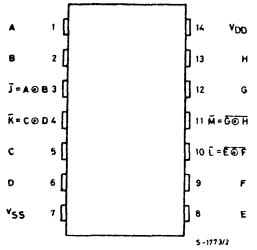


CONNECTION DIAGRAMS

for **4070B**



for **4077B**



TRUTH TABLES (1 of 4 gates)

for **4070B**

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where 1 = High level
0 = Low level
J = A ⊕ B

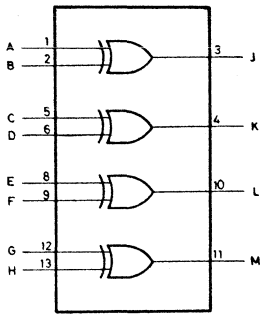
for **4077B**

A	B	$\bar{J}$
0	0	1
1	0	0
0	1	0
1	1	1

Where 1 = High level
0 = Low level
$\bar{J}$ = A ⊕ B

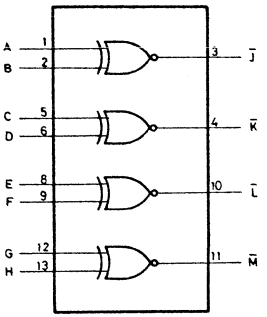
FUNCTIONAL DIAGRAMS

for **4070B**

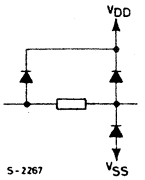


$J = A \oplus B$, $K = C \oplus D$, $L = E \oplus F$, $M = G \oplus H$
$V_{SS} = 7$, $V_{DD} = 14$ S-1770/1

for **4077B**



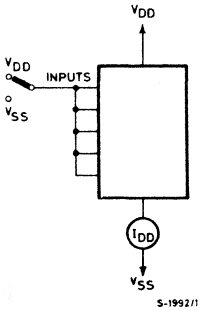
$\overline{J} = A \oplus B$, $\overline{K} = C \oplus D$, $\overline{L} = E \oplus F$, $\overline{M} = G \oplus H$
$V_{SS} = 7$, $V_{DD} = 14$ S-1771/1



ALL INPUTS PROTECTED BY COS/MOS PROTECTION NETWORK

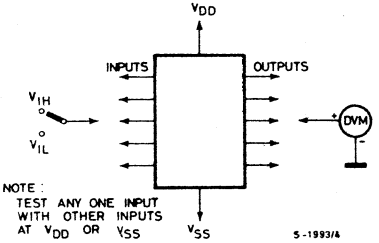
TEST CIRCUIT

Quiscent device current



S-1992/1

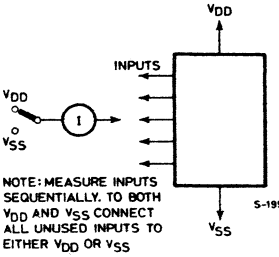
Input voltage



NOTE : TEST ANY ONE INPUT WITH OTHER INPUTS AT V_{DD} OR V_{SS}

S-1993/4

Input leakage current



NOTE: MEASURE INPUTS SEQUENTIALLY. TO BOTH V_{DD} AND V_{SS} CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}

S-1994/1

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

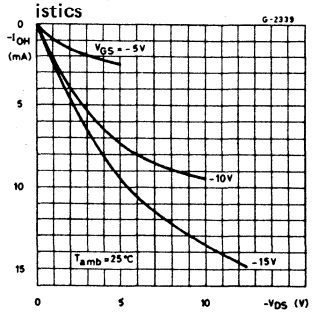
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

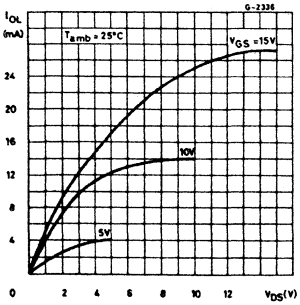
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
	V_{DD}(V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH} Propagation delay time	5		175	350	ns
	10		70	140	
	15		50	100	
t_{THL}, t_{TLH} Transition time	5		100	200	ns
	10		50	100	
	15		40	80	

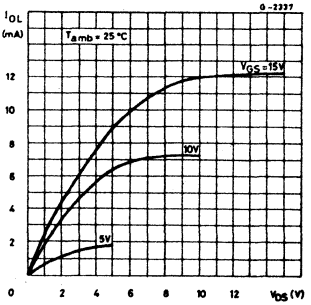
Minimum output high (source) current characteristics



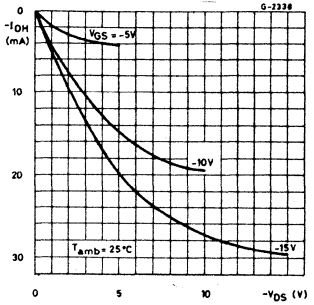
Typical output low (sink) current



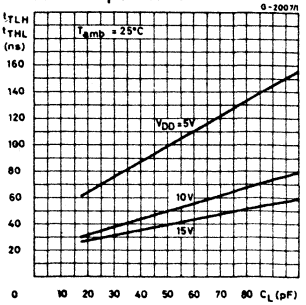
Minimum output low (sink) current characteristics



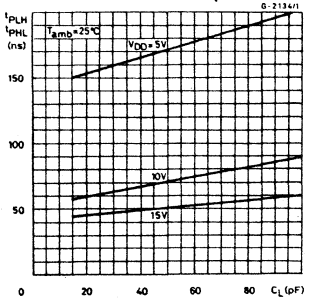
Typical output high (source) current characteristics



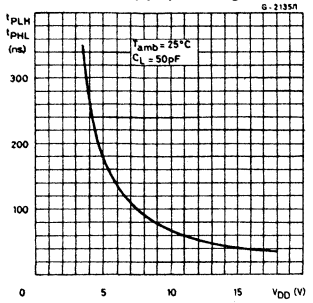
Typical transition time vs. load capacitance



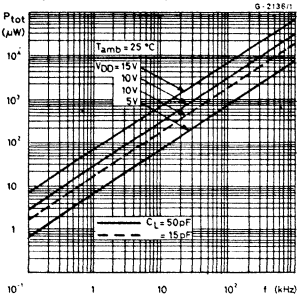
Typical propagation delay time vs. load capacitance



Typical propagation delay time vs. cupply voltage



Typical dynamic power dissipation vs. input frequency



COS/MOS INTEGRATED CIRCUITS

HCC/HCF 4071B
HCC/HCF 4072B
HCC/HCF 4075B

PRELIMINARY DATA

4071B - QUAD 2-INPUT OR GATE
4072B - DUAL 4-INPUT OR GATE
4075B - TRIPLE 3-INPUT OR GATE

- MEDIUM-SPEED OPERATION t_{PLH}, t_{PHL} = 60 ns. (TYP.) AT V_{DD} = 10V
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMP. RANGE)
- 5V, 10V AND 15V PARAMETRIC RATINGS

The **HCC 4071B/4072B** and **4075B** (extended temperature range) and **HCF 4071B/4072B** and **4075B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4071B, 4072B** and **4075B** OR gates provide the system designer with direct implementation of the positive-logic OR function and supplement the existing family of COS/MOS gates.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

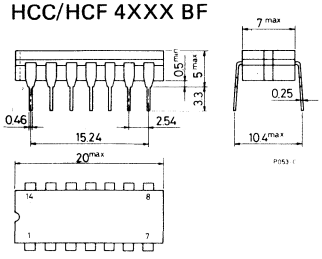
ORDERING NUMBERS:

HCC 40XX BD for dual in-line ceramic package
HCC 40XX BF for dual in-line ceramic package, frit seal
HCC 40XX BK for ceramic flat package
HCF 40XX BE for dual in-line plastic package
HCF 40XX BF for dual in-line ceramic package, frit seal

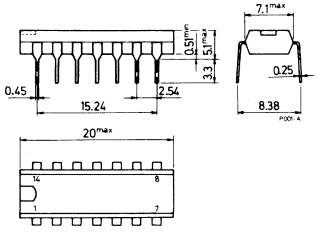
HCC/HCF 4071B
HCC/HCF 4072B
HCC/HCF 4075B

MECHANICAL DATA (dimensions in mm)

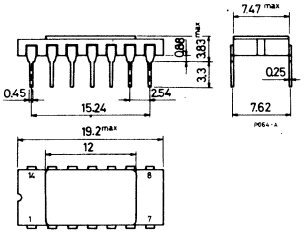
Dual in-line ceramic package for HCC/HCF 4XXX BF



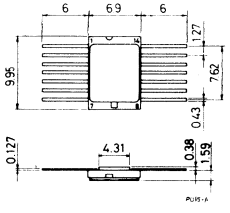
Dual in-line plastic package for HCF 4XXX BE



Dual in-line ceramic package for HCC 4XXX BD

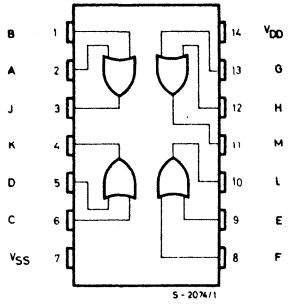


Ceramic flat package for HCC 4XXX BK

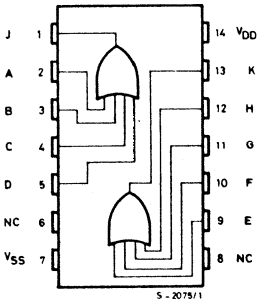


CONNECTION DIAGRAMS

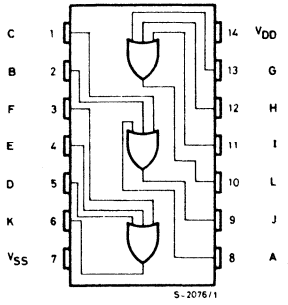
for **4071B**



for **4072B**



for **4075B**

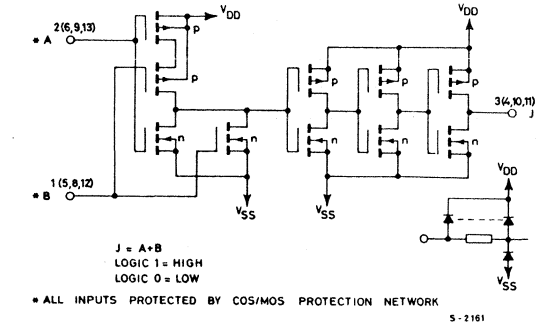


RECOMMENDED OPERATING CONDITIONS

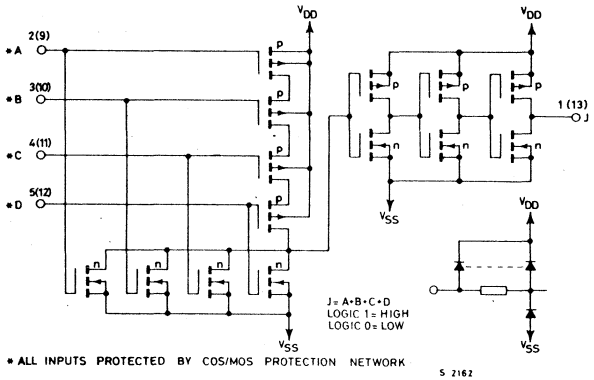
V_{DD}	Supply voltage	3 to 18	V
V_i	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

SCHEMATIC DIAGRAMS

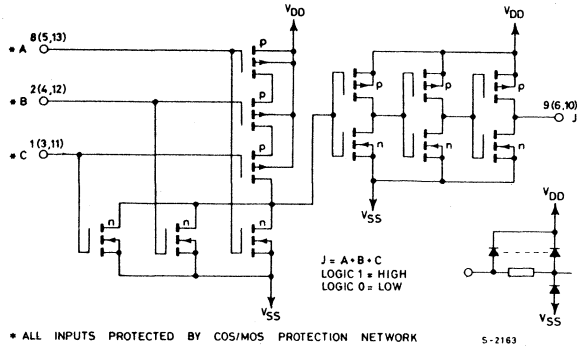
For **4071B** - 1 of 4 identical OR gates



For **4072B** - 1 of 2 identical OR gates



For **4075B** - 1 of 3 identical OR gates



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

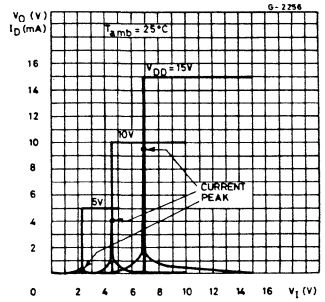
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				2/13	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13/2	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4,2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		±0.1		±10^{-5}	±0.1		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

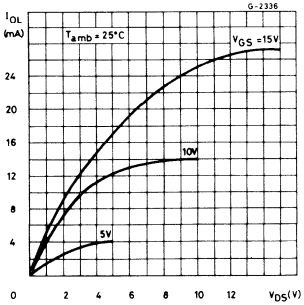
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD}= 0.3%/°C values, all input rise and fall time = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}	Propagation delay time	5		125	250	ns
		10		60	120	
		15		45	90	
t_{PLH}	Propagation delay time	5		175	350	ns
		10		70	140	
		15		50	110	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

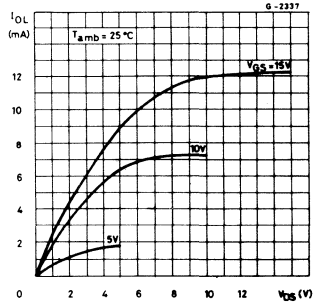
Typical voltage and current transfer characteristics



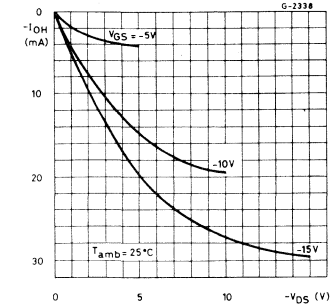
Typical output low (sink) current characteristics



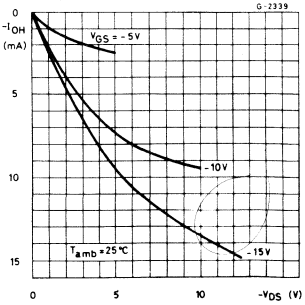
Minimum output low (sink) current characteristics



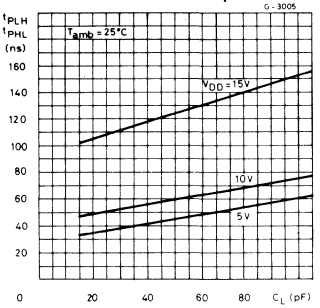
Typical output high (source) current characteristics



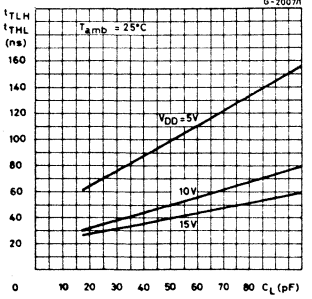
Minimum output high (source) current characteristics



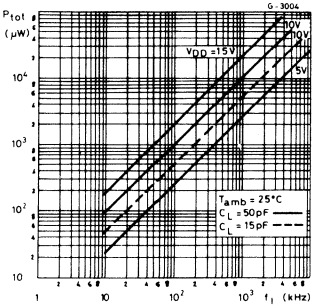
Typical propagation delay time vs. load capacitance



Typical transition time vs. load capacitance

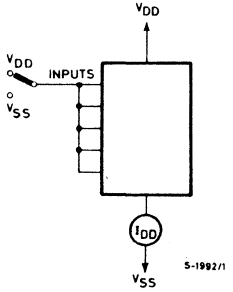


Typical dynamic power dissipation vs. frequency

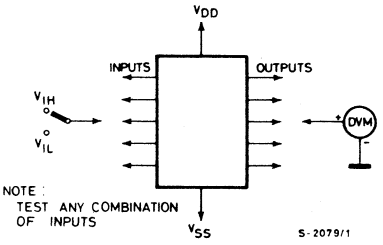


TEST CIRCUITS

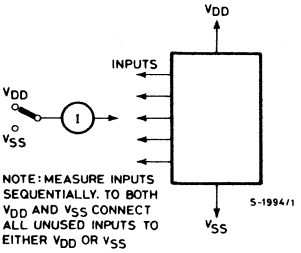
Quiescent device current



Input voltage



Input leakage current



COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4076 B

PRELIMINARY DATA

4-BIT D-TYPE REGISTERS

- THREE-STATE OUTPUTS
- INPUT DISABLED WITHOUT GATING THE CLOCK
- GATED OUTPUT CONTROL LINES FOR ENABLING OR DISABLING THE OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT LEAKAGE OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4076B** (extended temperature range) and **HCF 4076B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package.
The **HCC/HCF 4076B** types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

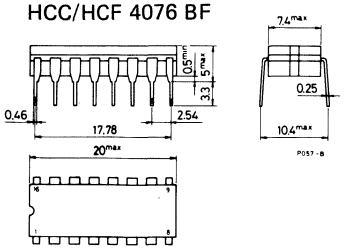
ORDERING NUMBERS:

HCC 4076 BD for dual in-line ceramic package
HCC 4076 BF for dual in-line ceramic package, frit seal
HCC 4076 BK for ceramic flat package
HCF 4076 BE for dual in-line plastic package
HCF 4076 BF for dual in-line ceramic package, frit seal

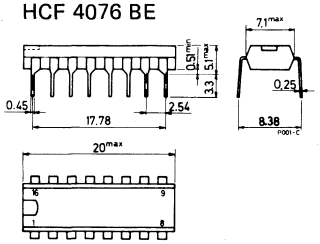
HCC/HCF 4076 B

MECHANICAL DATA (dimensions in mm)

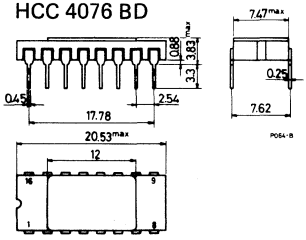
Dual in-line ceramic package for HCC/HCF 4076 BF



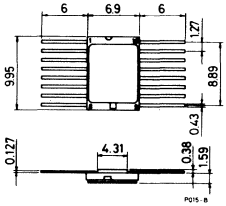
Dual in-line plastic package for HCF 4076 BE



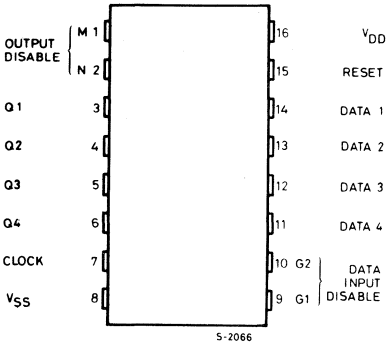
Dual in-line ceramic package for HCC 4076 BD



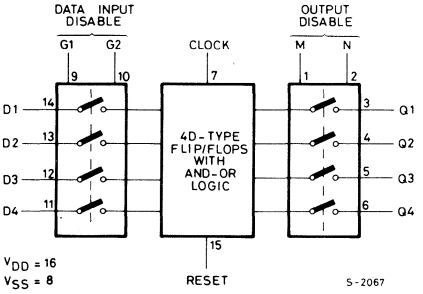
Ceramic flat package for HCC 4076 BK



CONNECTION DIAGRAM



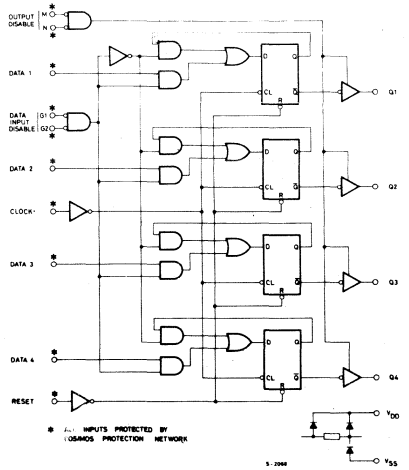
FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM



TRUTH TABLE

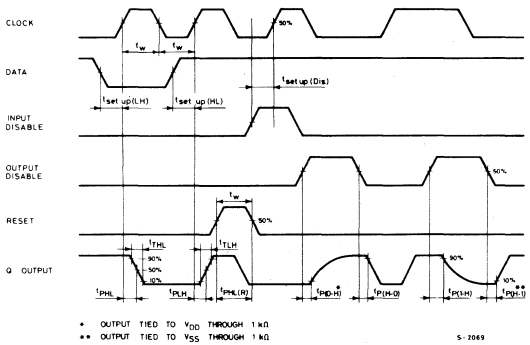
Reset	Clock	Data Input Disable G1	Data Input Disable G2	Data D	Next State Output Q	
1	X	X	X	X	0	
0	0	X	X	X	Q	NC
0	⌒	1	X	X	Q	NC
0	⌒	X	1	X	Q	NC
0	⌒	0	0	1	1	
0	⌒	0	0	0	0	
0	1	X	X	X	Q	NC
0	⌒	X	X	X	Q	NC

When either Output Disable M or N is high, the outputs are disabled (high impedance state); however sequential operation of the flip-flops is not affected.

1 ≡ High Level X = Don't Care

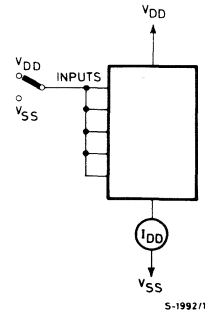
0 ≡ Low Level NC = No Change

WAVEFORMS

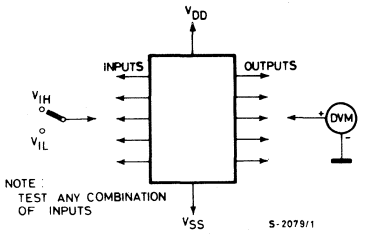


TEST CIRCUITS

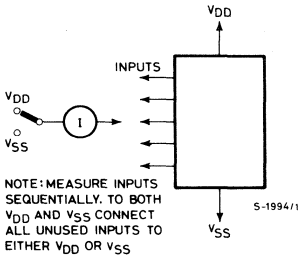
Quiescent device current



Noise immunity



Input leakage current



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

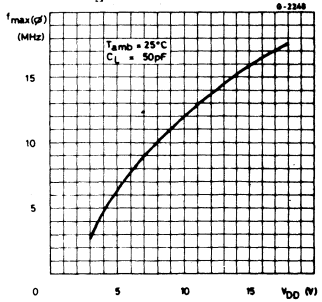
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
I_{OH},I_{OL}***	3-state output leakage current			0/18		18		±2		$\pm 10^{-4}$	±2		±20	μA
C_i**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input
*** Forced output disabled

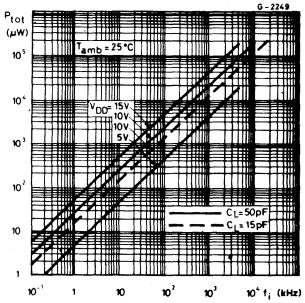
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time (clock to Q output)		5		300	600	ns
			10		125	250	
			15		90	180	
t_{PHL}(R)	Propagation delay time (Reset)		5		230	460	ns
			10		100	200	
			15		75	150	
$t_{P(1-H)}$, $t_{P(0-H)}$	3-state output 1 or 0 to high impedance	R_L= 1 kΩ	5		150	300	ns
			10		75	150	
			15		60	120	
$t_{P(H-1)}$, $t_{P(H-0)}$	3-state high impedance to 1 or 0 output	R_L= 1 kΩ	5		150	300	ns
			10		75	150	
			15		60	120	
t_{TLH}, t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
t_W	Clock pulse width		5	200	100		ns
			10	100	50		
			15	80	40		
t_W	Reset pulse width		5	120	60		ns
			10	50	25		
			15	40	20		
t_{setup}	Data setup time		5	200	100		ns
			10	80	40		
			15	60	30		
t_{setup}	Data input disable setup time		5	180	90		ns
			10	100	50		
			15	70	35		
f_{max}	Maximum clock frequency		5	3	6		MHz
			10	6	12		
			15	8	16		

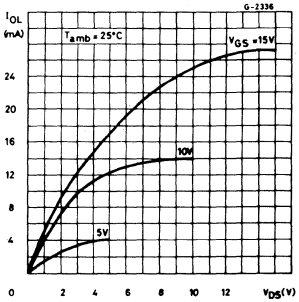
Typical maximum clock input frequency vs. supply voltage



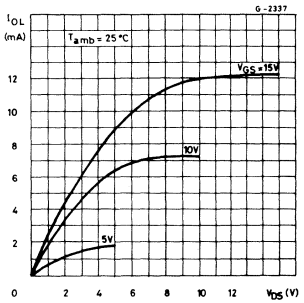
Typical dynamic power dissipation vs. frequency



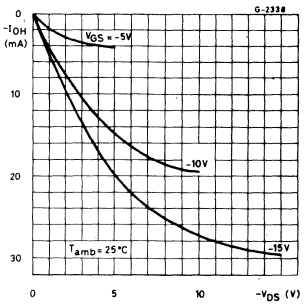
Typical output low (sink) current characteristics



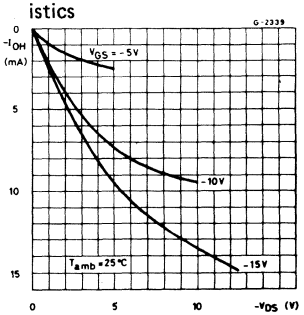
Minimum output low (sink) current characteristics



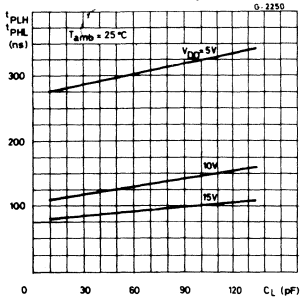
Typical output high (source) current characteristics



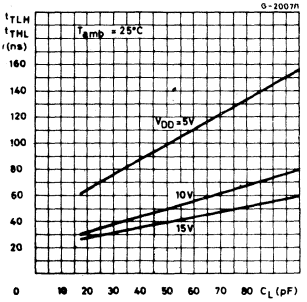
Minimum output high (source) current characteristics



Typical propagation delay time vs. load capacitance



Typical transition time vs. load capacitance



COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4078B

PRELIMINARY DATA

8-INPUT NOR/OR GATE

- MEDIUM-SPEED OPERATION t_{PHL}, t_{PLH} = 75 ns (TYP.) AT V_{DD}= 10V
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT LEAKAGE CURRENT OF 1 μA AT 18V (FULL-PACKAGE TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4078B** (extended temperature range) and **HCF 4078B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package, and ceramic flat package.
The **HCC/HCF 4078B** NOR/OR Gate provides the system designer with direct implementation of the positive-logic-8-input NOR and OR function and supplements the existing family of COS/MOS gates.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

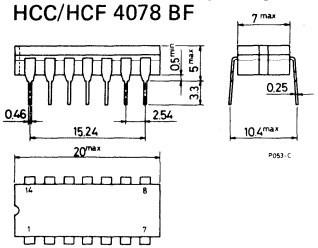
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

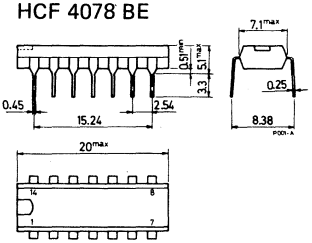
HCC 4078 BD for dual in-line ceramic package
HCC 4078 BF for dual in-line ceramic package, frit seal
HCC 4078 BK for ceramic flat package
HCF 4078 BE for dual in-line plastic package
HCF 4078 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

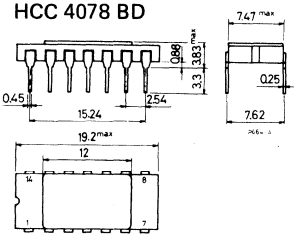
Dual in-line ceramic package for HCC/HCF 4078 BF



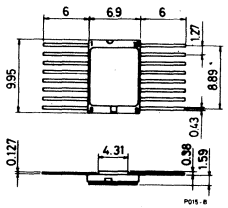
Dual in-line plastic package for HCF 4078 BE



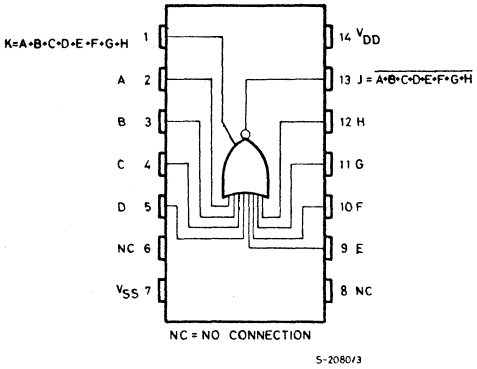
Dual in-line ceramic package for HCC 4078 BD



Ceramic flat package for HCC 4078 BK



CONNECTION DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

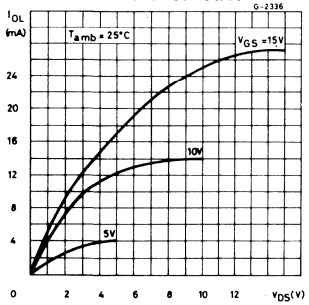
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		±0.1		±10^{-5}	±0.1		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

T_{Low}= - 55°C for **HCC** device; - 40°C for **HCF** device.
T_{High}= +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

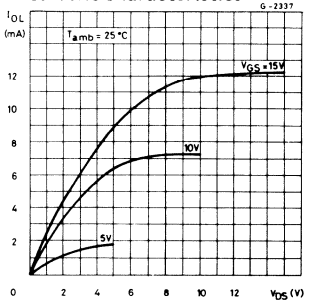
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25 °C, C_L= 50 pF, R_L= 200 KΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall time = 20 ns)

Parameter	Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH} Propagation delay time		5		150	300	ns
		10		75	150	
		15		55	110	
t_{THL}, t_{TLH} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	

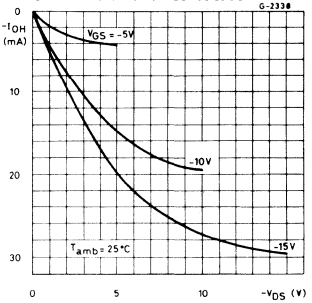
Typical output low (sink) current characteristics



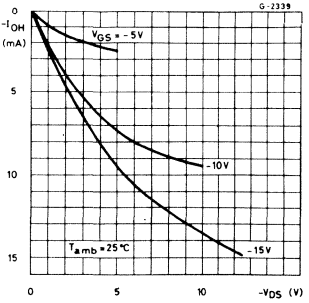
Minimum output low (sink) current characteristics



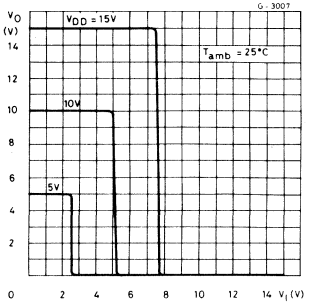
Typical output high (source) current characteristics



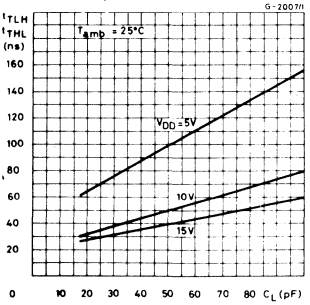
Minimum output high (source) current characteristics



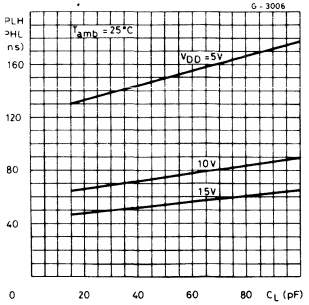
Typical voltage transfer characteristics(NOR output)



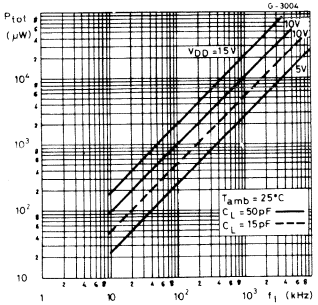
Typical transition time vs. load capacitance



Typical propagation delay time vs, load capacitance

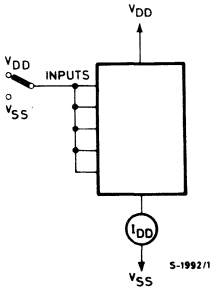


Typical power dissipation vs. frequency

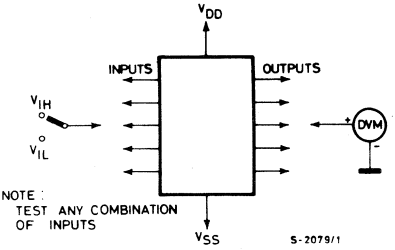


TEST CIRCUITS

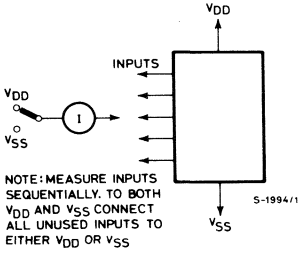
Quiescent device current



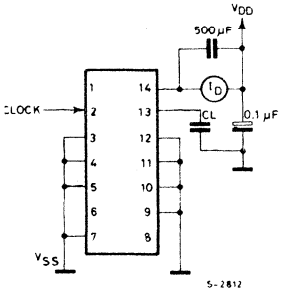
Input voltage



Input current



Dynamic power dissipation



COS/MOS INTEGRATED CIRCUITS

HCC/HCF 4081 B
HCC/HCF 4082B
HCC/HCF 4073B

PRELIMINARY DATA

COS/MOS AND GATES: **4081B QUAD 2 - INPUT AND GATE**
4082B DUAL 4 - INPUT AND GATE
4073B TRIPLE 3 - INPUT AND GATE

- MEDIUM SPEED OPERATION - t_{PLH}= 85 ns (TYP.); t_{PHL}= 65 ns (TYP.) AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT LEAKAGE CURRENT 1 μA AT 18V (FULL PACKAGE-TEMP. RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4081B, HCC 4082B** and **HCC 4073B** (extended temperature range) and the **HCF 4081B, HCF 4082B** and **HCF 4073B** (intermediate temperature range) are monolithic integrated circuits available in 14-lead dual in-line plastic or ceramic package, and ceramic flat package. The **HCC/HCF 4081B, 4082B** and **4073B** AND gates provide the system designer with direct implementation of the AND function and supplement the existing family of COS/MOS gates.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

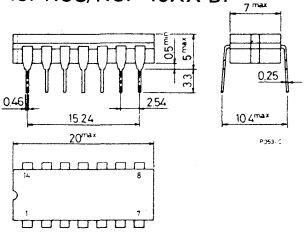
ORDERING NUMBERS:

HCC 40XX BD for dual in-line ceramic package
HCC 40XX BF for dual in-line ceramic package frit seal, (extended temperature range)
HCC 40XX BK for ceramic flat package
HCF 40XX BE for dual in-line plastic package
HCF 40XX BF for dual in-line ceramic package frit seal, (intermediate temperature range)

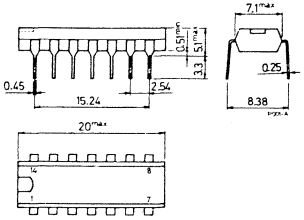
HCC/HCF 4081 B
HCC/HCF 4082B
HCC/HCF 4073B

MECHANICAL DATA (dimensions in mm)

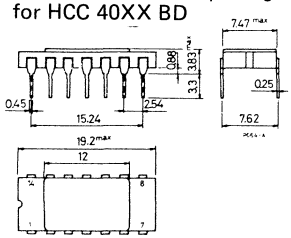
Dual in-line ceramic package
for HCC/HCF 40XX BF



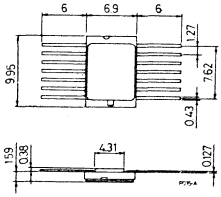
Dual in-line plastic package
for HCF 40XX BE



Dual in-line ceramic package
for HCC 40XX BD

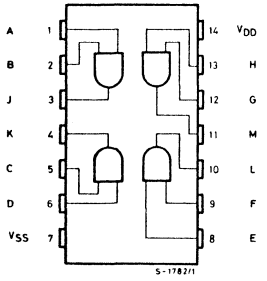


Ceramic flat package
for HCC 40XX BK

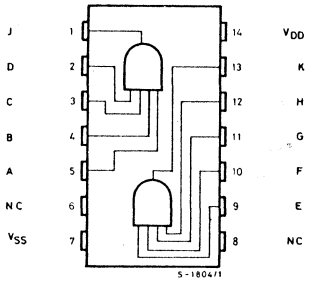


CONNECTION DIAGRAMS

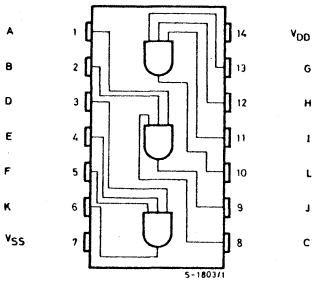
For **4081B**



For **4082B**



For **4073B**



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

TATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

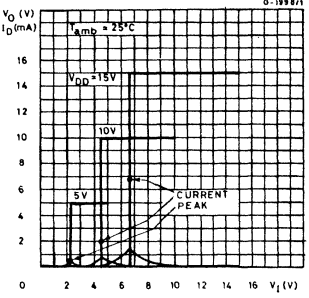
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		0.25		0.01	0.25		7.5	μA
			0/10			10		0.5		0.01	0.5		15	
			0/15			15		1		0.01	1		30	
			0/20			20		5		0.02	5		150	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				2/13	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13/2	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}	Input leakage current		0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

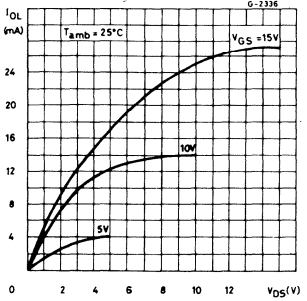
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns, R_L = 200 kΩ)

Parameter	Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH} Propagation delay time		5		125	250	ns
		10		60	125	
		15		45	90	
t_{TLH}, t_{THL} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	

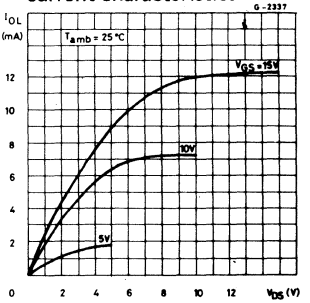
Typical voltage and current transfer characteristics



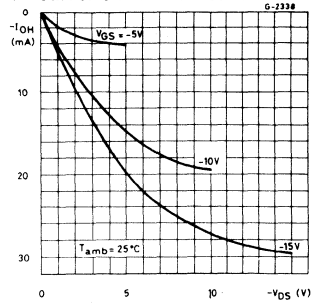
Typical output low (sink) current



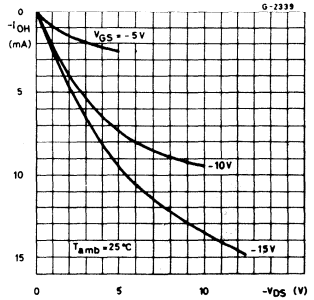
Minimum output low (sink) current characteristics



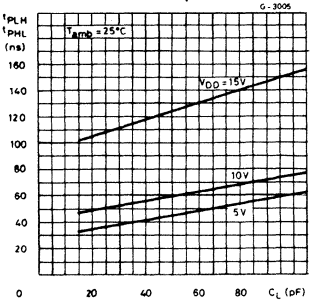
Typical output high (source) current characteristics



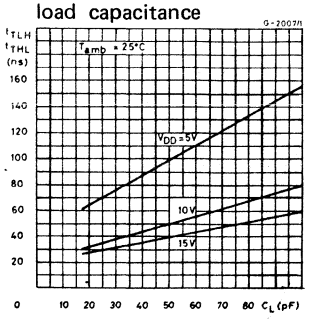
Minimum output high (source) current characteristics



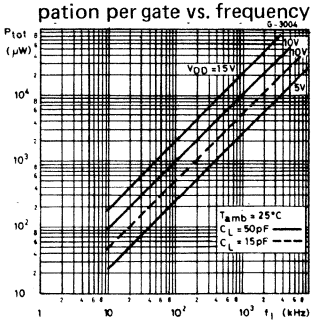
Typical propagation delay time vs. load capacitance



Typical transition time vs. load capacitance

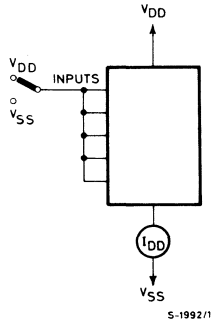


Typical dynamic power dissipation per gate vs. frequency

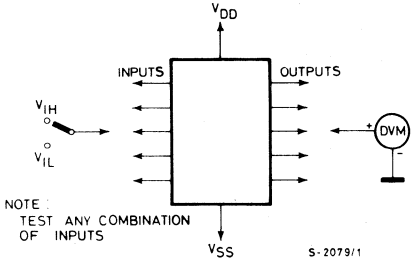


TEST CIRCUITS

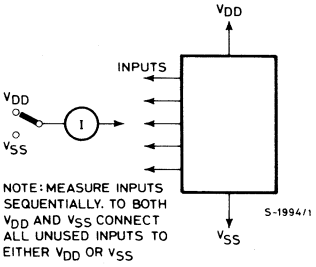
Quiescent device current



Input voltage



Input leakage current



COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4085 B

PRELIMINARY DATA

DUAL 2-WIDE 2-INPUT AND-OR-INVERTER GATE

- MEDIUM-SPEED OPERATION - t_{PHL}= 90 ns; t_{PLH}= 125 ns (TYP.) AT 10V
- INDIVIDUAL INHIBIT CONTROLS
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4085B** (extended temperature range) and **HCF 4085B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4085B** contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. Individual inhibit controls are provided for both A-O-I gates.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

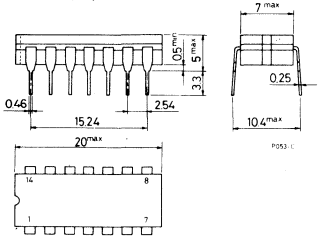
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

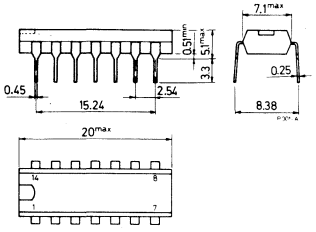
HCC 4085 BD for dual in-line ceramic package
HCC 4085 BF for dual in-line ceramic package, frit seal
HCC 4085 BK for ceramic flat package
HCF 4085 BE for dual in-line plastic package
HCF 4085 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

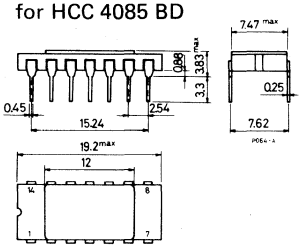
Dual in-line ceramic package
for HCC/HCF 4085 BF



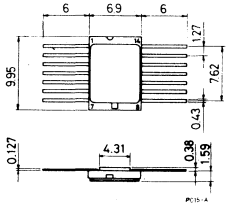
Dual in-line plastic package
for HCF 4085 BE



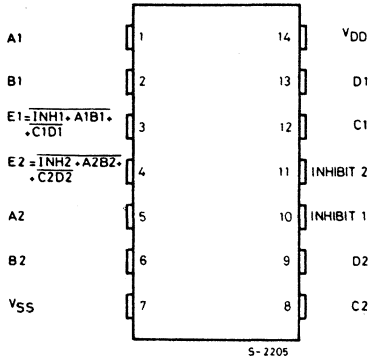
Dual in-line ceramic package
for HCC 4085 BD



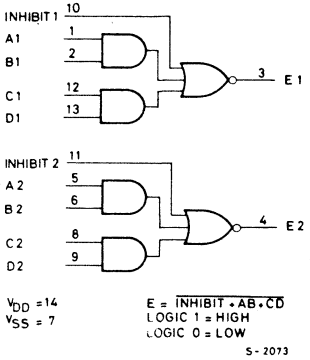
Ceramic flat package
for HCC 4085 BK



CONNECTION DIAGRAM



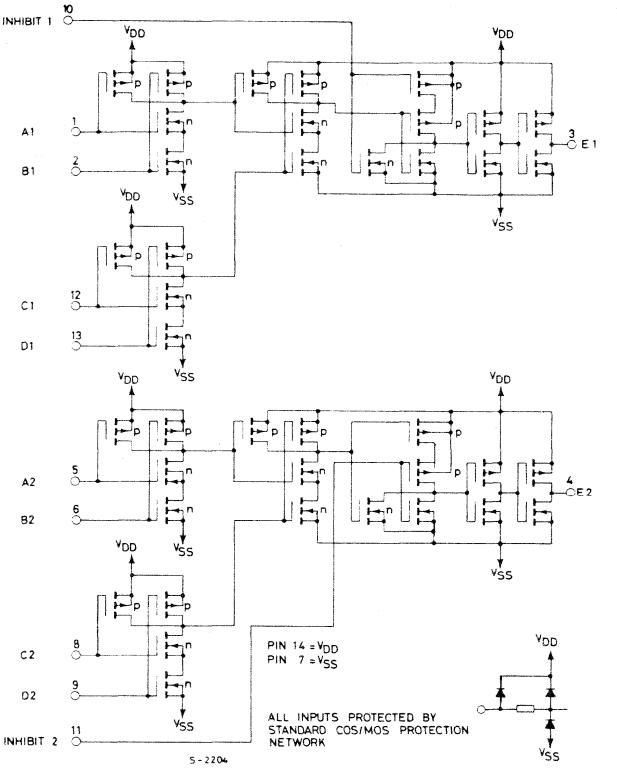
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

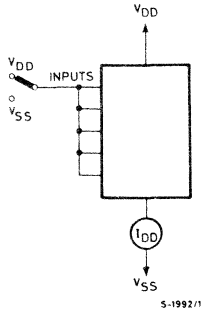
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

SCHEMATIC DIAGRAM

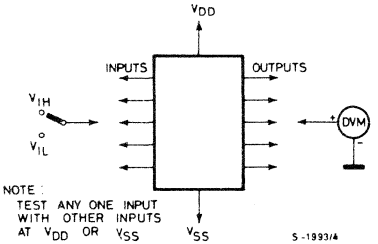


TEST CIRCUITS

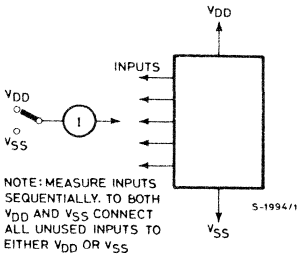
Quiescent device current



Input voltage



Input current



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

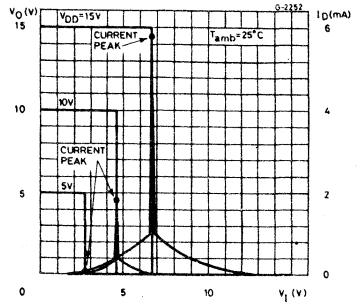
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		V
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		V
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		±0.1		±10^{-5}	±0.1		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

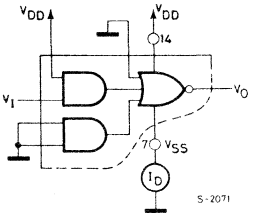
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

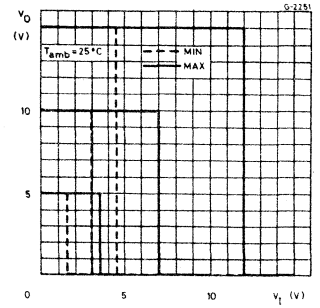
Parameter		Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}	Propagation delay time (Data)		5		225	450	ns
			10		90	180	
			15		65	130	
t_{PLH}	Propagation delay time (Data)		5		310	620	
			10		125	250	
			15		90	180	
t_{PHL}	Propagation delay time (Inhibit)		5		150	300	ns
			10		60	120	
			15		40	80	
t_{PLH}	Propagation delay time (Inhibit)		5		250	500	
			10		100	200	
			15		70	140	
t_{TLH}, t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	

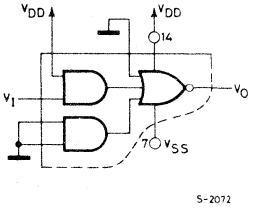
Typical voltage and current transfer characteristics with test circuit



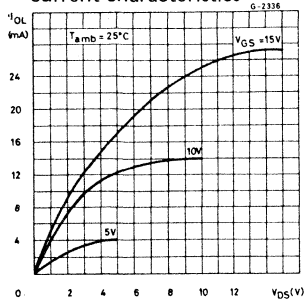


Minimum and maximum voltage transfer characteristics with test circuit

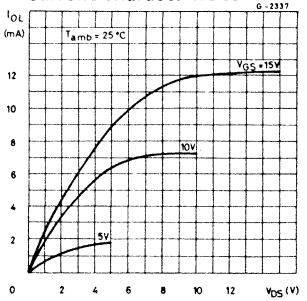




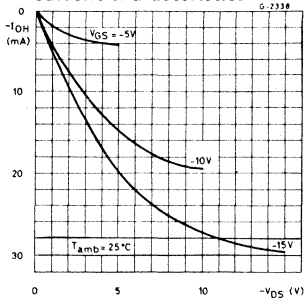
Typical output low (sink) current characteristics



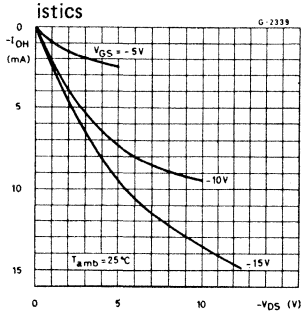
Minimum output low (sink) current characteristics



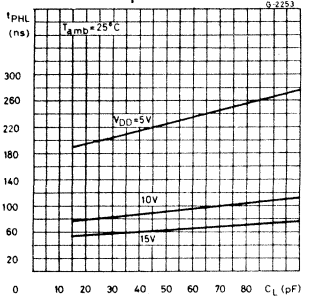
Typical output high (source) current characteristics



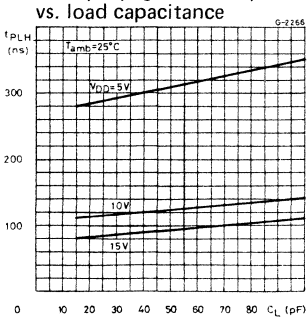
Minimum output high (source) current characteristics



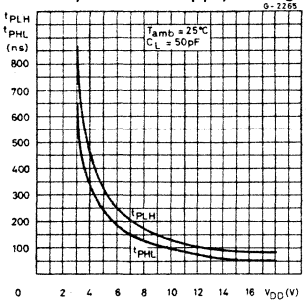
Typical data high-to-low level propagation delay time vs. load capacitance



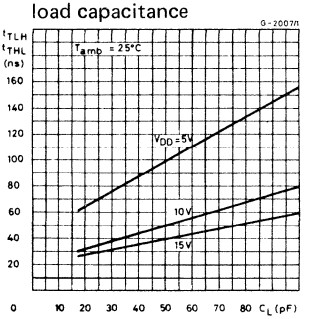
Typical data low-to-high level propagation delay time vs. load capacitance



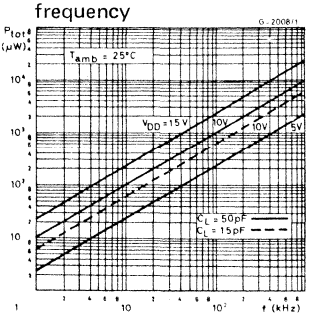
Typical data propagation delay time vs. supply voltage



Typical transition time vs. load capacitance



Typical power dissipation vs. frequency



COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4086B

PRELIMINARY DATA

EXPANDABLE 4-WIDE 2-INPUT AND-OR-INVERT GATE

- MEDIUM-SPEED OPERATION-- t_{PHL}= 90 ns; t_{PLH}= 140 ns (TYP.) AT 10V
- INHIBIT AND ENABLE INPUTS
- BUFFERED OUTPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT LEAKAGE CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4086B** (extended temperature range) and **HCF 4086B** (intermediate temperature range) are monolithic integrated circuit, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4086B** contains one 4-wide 2-input AND-OR-INVERT gate with an INHIBIT/$\overline{EXP}$ input and an ENABLE/EXP input. For a 4-wide A-O-I function INHIBIT/$\overline{EXP}$ is tied to V_{SS} and ENABLE/EXP to V_{DD}. See application and its associated explanation for applications where a capability greater than 4-wide is required.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

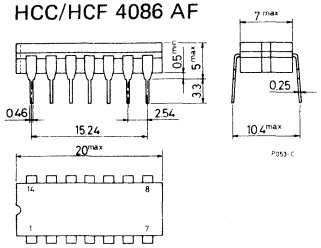
ORDERING NUMBERS:

HCC 4086 BD for dual in-line ceramic package
HCC 4086 BF for dual in-line ceramic package, frit seal
HCC 4086 BK for ceramic flat package
HCF 4086 BE for dual in-line plastic package
HCF 4086 BF for dual in-line ceramic package, frit seal

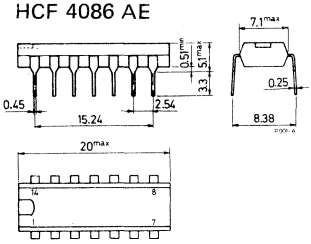
HCC/HCF 4086B

MECHANICAL DATA (dimensions in mm)

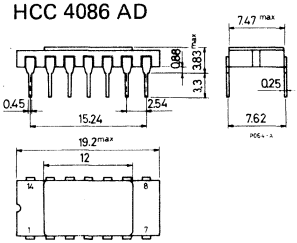
Dual in-line ceramic package for HCC/HCF 4086 AF



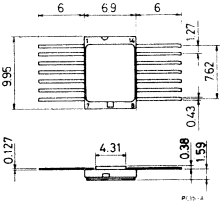
Dual in-line plastic package for HCF 4086 AE



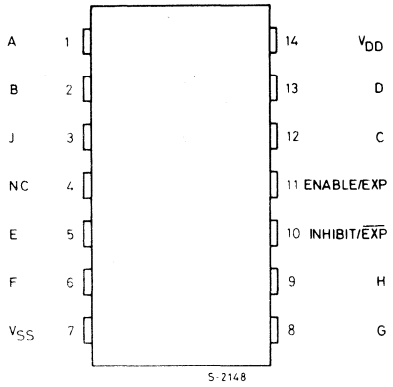
Dual in-line ceramic package for HCC 4086 AD



Ceramic flat package for HCC 4086 AK



CONNECTION DIAGRAM



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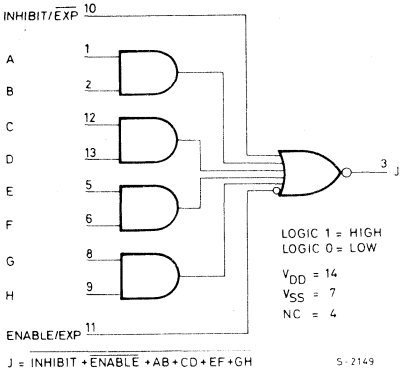
FUNCTIONAL DIAGRAM



$J = \overline{\text{INHIBIT} + \text{ENABLE}} + AB + CD + EF + GH$

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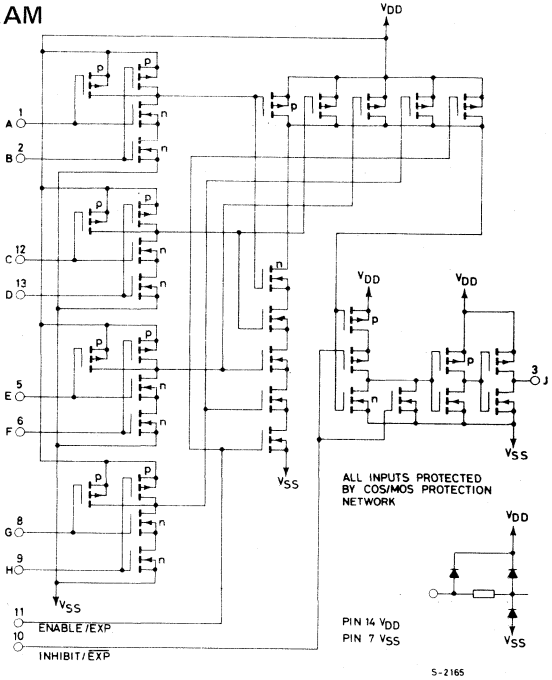
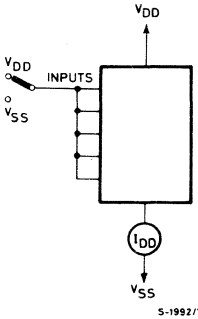
SCHEMATIC DIAGRAM

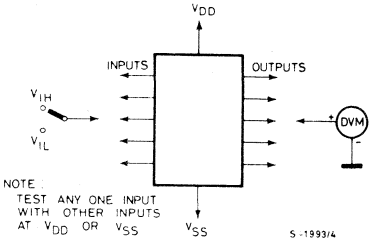


TEST CIRCUITS

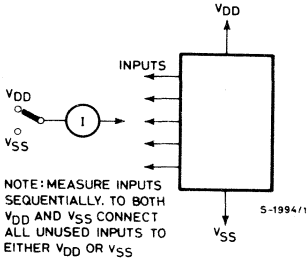
Quiescent device current



Input voltage



Input leakage current



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

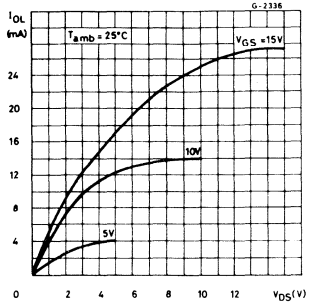
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		±0.1		±10^{-5}	±0.1		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = − 55°C for **HCC** device; − 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

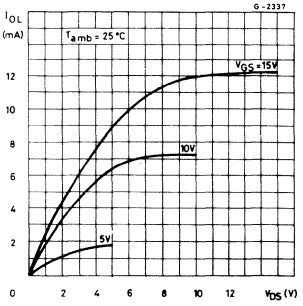
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}	Propagation delay time (Data)	5		225	450	ns
		10		90	180	
		15		60	120	
t_{PLH}	Propagation delay time (Data)	5		350	700	
		10		140	280	
		15		100	200	
t_{PHL}	Propagation delay time (Inhibit)	5		150	300	ns
		10		60	120	
		15		40	80	
t_{PLH}	Propagation delay time (Inhibit)	5		250	500	
		10		100	200	
		15		70	140	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	

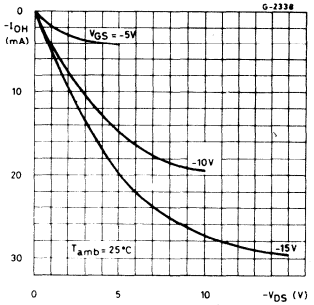
Typical output low (sink) current characteristics



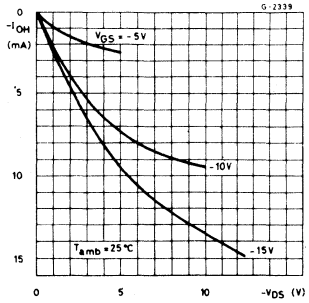
Minimum output low (sink) current characteristics



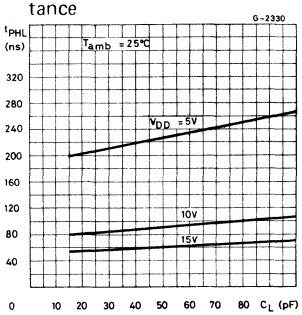
Typical output high (source) current characteristics



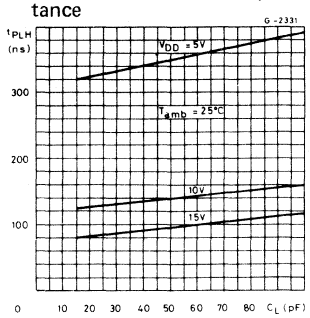
Minimum output high (source) current characteristics



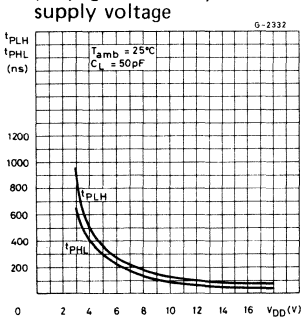
Typical DATA or ENABLE high-to-low level propagation delay time vs. load capacitance



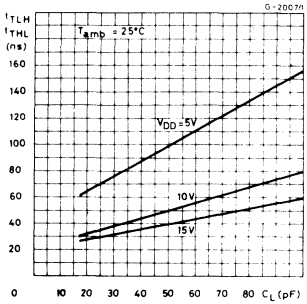
Typical DATA or ENABLE low-to-high level propagation delay time vs. load capacitance



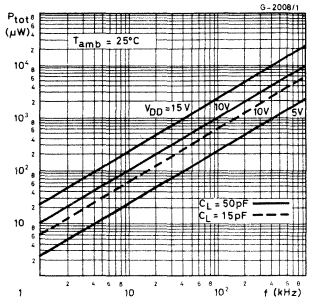
Typical DATA or ENABLE propagation delay time vs. supply voltage



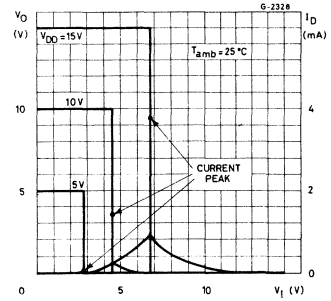
Typical transition time vs. load capacitance

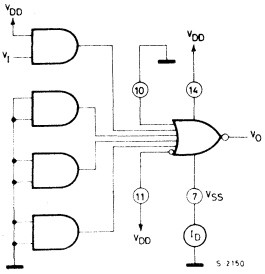


Typical power dissipation vs. frequency

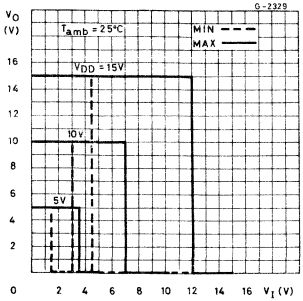


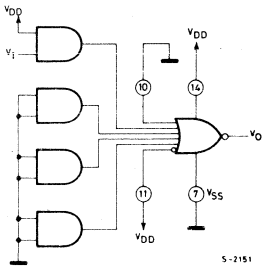
Typical voltage and current transfer characteristics and test circuit





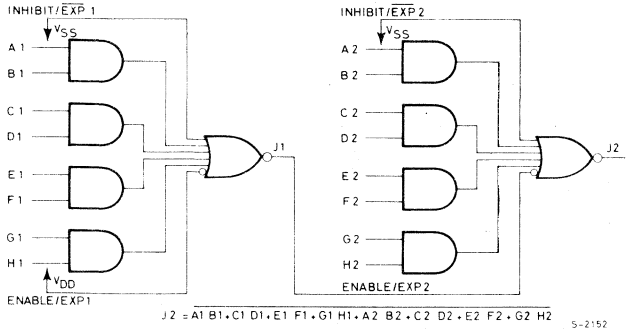
Minimum and maximum voltage transfer characteristics and test circuit





APPLICATION

Two 4086B connected as an 8-wide 2-input A-O-I gate



This application shows two **HCC/HCF 4086B** utilized to obtain an 8-wide 2-input A-O-I function. The output (J1) of one **HCC/HCF 4086B** is fed directly to the ENABLE/EXP 2 line of the second **HCC/HCF 4086B**. In a similar fashion, any NAND gate output can be fed directly into the ENABLE/EXP input to obtain a 5-wide A-O-I function. In addition, any AND gate output can be fed directly into the INHIBIT/$\overline{EXP}$ input with the same result.

COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4089B

PRELIMINARY DATA

BINARY RATE MULTIPLIER

- CASCADABLE IN MULTIPLES OF 4-BITS
- SET TO "15" INPUT AND "15" DETECT OUTPUT
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS

The **HCC 4089B** (extended temperature range) and **HCF 4089B** (intermediate temperature range) are monolithic integrated circuit available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package.
The **HCC/HCF 4089B** is a low-power 4-bit digital rate multiplier that provides an output pulse rate that is the clock-input-pulse rate multiplied by 1/16 times the binary input. For example, when the binary input number is 13, there will be 13 output pulses for every 16 input pulses.
The **HCC/HCF 4089B** has an internal synchronous 4-bit counter which, together with one of the four binary input bits, produces pulse trains as shown in timing diagram.
If more than one binary input bit is high, the resulting pulse train is a combination of the above separate pulse trains. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversions, and frequency division.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

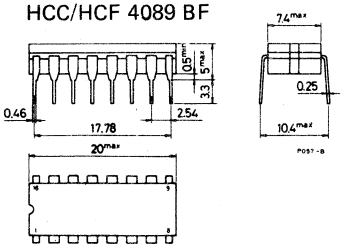
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

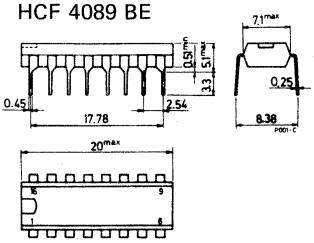
HCC 4089 BD for dual in-line ceramic package
HCC 4089 BF for dual in-line ceramic package, frit seal
HCC 4089 BK for ceramic flat package
HCF 4089 BE for dual in-line plastic package
HCF 4089 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

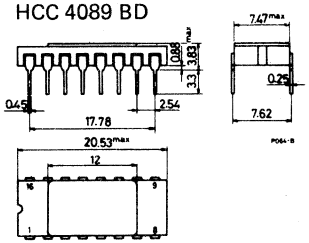
Dual in-line ceramic package for HCC/HCF 4089 BF



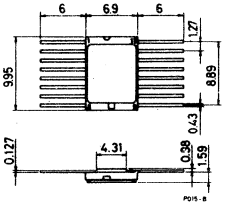
Dual in-line plastic package for HCF 4089 BE



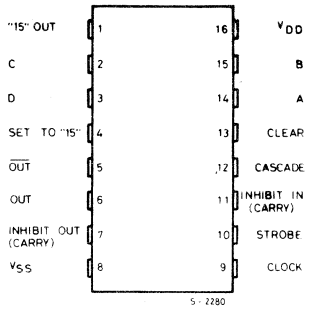
Dual in-line ceramic package for HCC 4089 BD



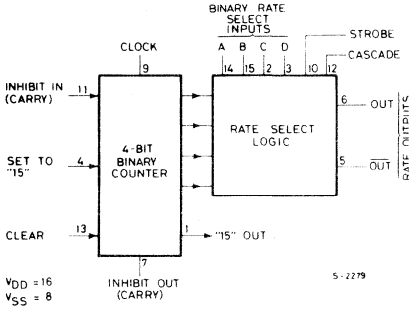
Ceramic flat package for HCC 4089 BK



CONNECTION DIAGRAM



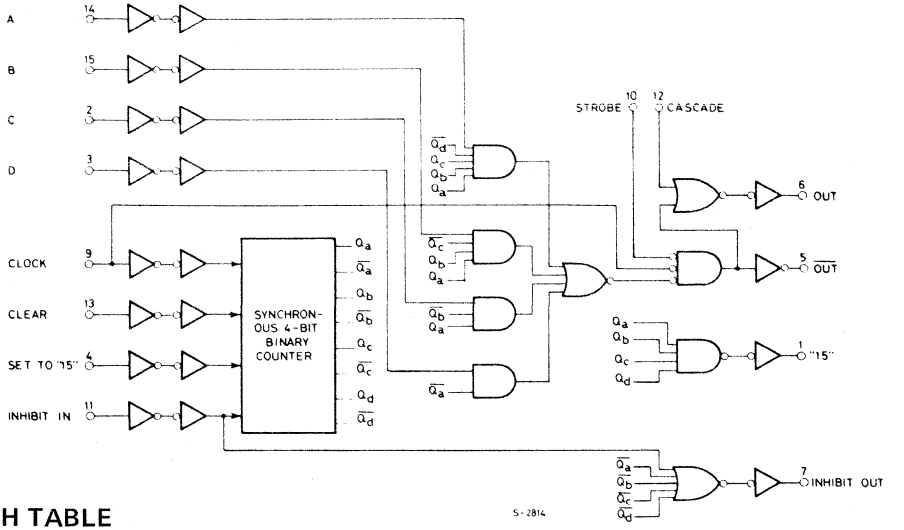
FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM



TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{OUT}$	INH OUT	"15" OUT
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	●	●	H	●
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	0	1	L	H	L	H

* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).
● Depends on internal state of counter.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

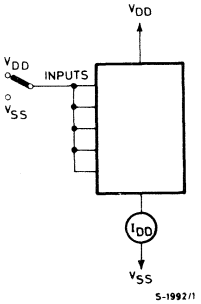
Parameter		Test conditions	V_{DD} (V)	Values Min.	Typ.	Max.	Unit
t_{PHL}, t_{PLH} Propagation delay time	Clock to out		5		110	220	ns
			10		55	110	
			15		45	90	
	Clock or strobe to out		5		150	300	ns
			10		75	150	
			15		60	120	
	Clock to inhibit high level to low level		5		360	720	ns
			10		160	320	
			15		110	220	
	Low level to high level		5		250	500	ns
			10		100	200	
			15		75	150	
	Clear to out		5		380	760	ns
			10		175	350	
			15		130	260	
	Clock to "9" or "15" out		5		300	600	ns
			10		125	250	
			15		90	180	
	Cascade to out		5		90	180	ns
			10		45	90	
			15		35	70	
	Inhibit in to inhibit out		5		160	320	ns
			10		75	150	
			15		55	110	
	Set to out		5		330	660	ns
			10		150	300	
			15		110	220	
t_{THL}, t_{TLH} Transition time			5		100	200	ns
			10		50	100	
			15		40	80	
f_{CL} Maximum clock frequency			5	1.2	2.4		MHz
			10	2.5	5		
			15	3.5	7		
t_W Clock pulse width			5	330	165		ns
			10	170	85		
			15	100	50		
t_r, t_f Clock rise or fall time			5			15	μs
			10			15	
			15			15	
t_W Set or clear pulse width			5	160	80		ns
			10	90	45		
			15	60	30		

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

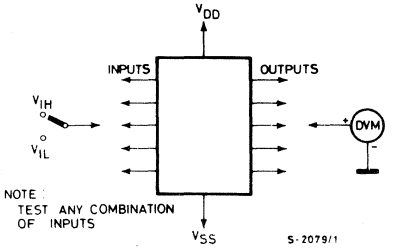
Parameter		Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{setup}	Inhibit input setup time, high level to low level		5	100	50		ns
			10	40	20		
			15	20	10		
t_R	Inhibit, input removal time		5	240	120		ns
			10	130	65		
			15	110	55		
t_R	Minimum set removal time		5	150	75		ns
			10	80	40		
			15	50	25		
t_R	Clear removal time		5	60	30		ns
			10	40	20		
			15	30	15		

TEST CIRCUIT

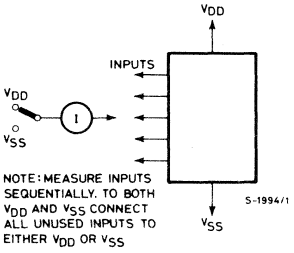
Quiescent device current



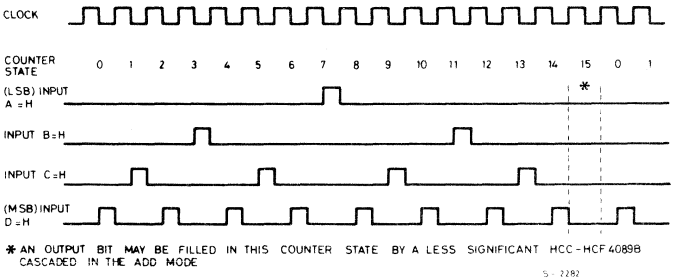
Noise immunity



Input leakage current



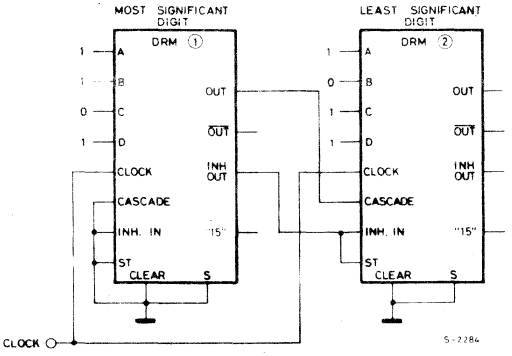
TIMING DIAGRAM



APPLICATION NOTES

For words of more than 4 bits, **HCC/HCF 4089B** devices may be cascaded in two different modes: an Add mode and a Multiply mode.

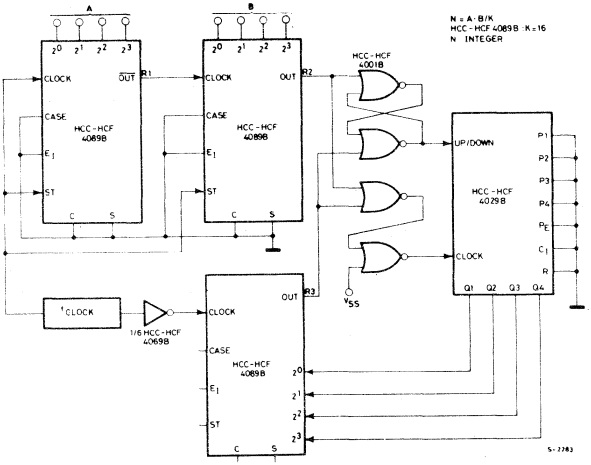
Two **HCC/HCF 4089B**'s cascaded in the "Add" mode with a preset number of 189.



Nota:
In the Add mode some of the gaps left by the more significant unit at the count of 15 are filled in by the less significant units. For example, when two units are cascaded in the Add mode and programmed to 11 and 13, respectively, the more significant unit will have 11 output pulses for every 16 input pulses and the other unit will have 13 output pulses for every 256 input pulses for a total of

$$\frac{11}{16} + \frac{13}{256} = \frac{189}{256}$$

Two **HCC/HCF 4089B**'s cascaded in the Multiply mode for Multiplication of two variables A and B with loop circuit control.



When the loop stabilises rate R_2= rate R_3, thus $f_{clock}\ (\frac{A}{16} \cdot \frac{B}{16}) = f_{clock}\ (\frac{1}{16} \cdot \frac{N}{16})$ therefore $N = A \cdot B$.

COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

QUAD 2-INPUT NAND SCHMITT TRIGGERS

- SCHMITT-TRIGGER ACTION ON EACH INPUT WITH NO EXTERNAL COMPONENTS
- HYSTERESIS VOLTAGE TYPICALLY 0.9V AT V_{DD}= 5V AND 2.3V AT V_{DD}= 10V
- NOISE IMMUNITY GREATER THAN 50% OF V_{DD} (TYP.)
- NO LIMIT ON INPUT RISE AND FALL TIMES
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4093B** (extended temperature range) and **HCF 4093B** (intermediate temperature range) are available in 14-lead dual in-line plastic or ceramic package, and ceramic flat package.
The **HCC/HCF 4093B** consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals.
The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H) (See Fig. 1).

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

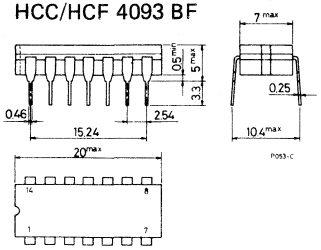
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

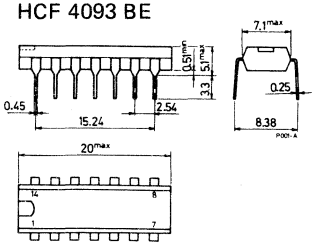
HCC 4093 BD	for dual in-line ceramic package
HCC 4093 BF	for dual in-line ceramic package, frit seal
HCC 4093 BK	for ceramic flat package
HCF 4093 BE	for dual in-line plastic package
HCF 4093 BF	for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

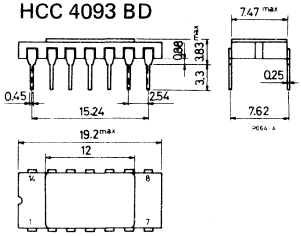
Dual in-line ceramic package for HCC/HCF 4093 BF



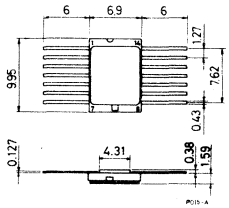
Dual in-line plastic package for HCF 4093 BE



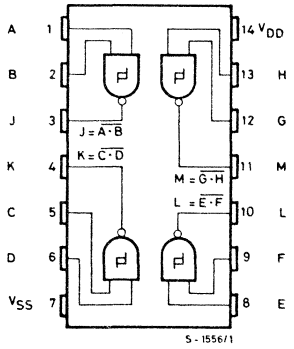
Dual in-line ceramic package for HCC 4093 BD



Ceramic flat package for HCC 4093 BK

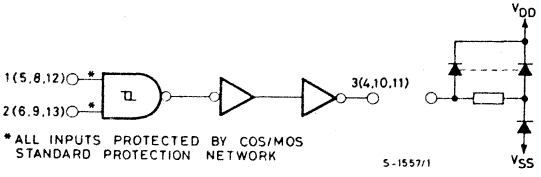


CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

1 of 4 Schmitt triggers



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		Test conditions				Values							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
						Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
		0/10			10		2		0.02	2		60	
		0/15			15		4		0.02	4		120	
		0/20			20		20		0.04	20		600	
V_P Positive trigger threshold voltage		a			5	2.2	3.6	2.2	2.9	3.6	2.2	3.6	V
		a			10	4.6	7.1	4.6	5.9	7.1	4.6	7.1	
		a			15	6.8	10.8	6.8	8.8	10.8	6.8	10.8	
		b			5	2.6	4	2.6	3.3	4	2.6	4	
		b			10	5.6	8.2	5.6	7	8.2	5.6	8.2	
		b			15	6.3	12.7	6.3	9.4	12.7	6.3	12.7	
V_N Negative trigger threshold voltage		a			5	0.9	2.8	0.9	1.9	2.8	0.9	2.8	V
		a			10	2.5	5.2	2.5	3.9	5.2	2.5	5.2	
		a			15	4	7.4	4	5.8	7.4	4	7.4	
		b			5	1.4	3.2	1.4	2.3	3.2	1.4	3.2	
		b			10	3.4	6.6	3.4	5.1	6.6	3.4	6.6	
		b			15	4.8	9.6	4.8	7.3	9.6	4.8	9.6	
V_H Hysteresis voltage		a			5	0.3	1.6	0.3	0.9	1.6	0.3	1.6	V
		a			10	1.2	3.4	1.2	2.3	3.4	1.2	3.4	
		a			15	1.6	5	1.6	3.5	5	1.6	5	
		b			5	0.3	1.6	0.3	0.9	1.6	0.3	1.6	
		b			10	1.2	3.4	1.2	2.3	3.4	1.2	3.4	
		b			15	1.6	5	1.6	3.5	5	1.6	5	
V_{OH} Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
		0/10		< 1	10	9.95		9.95			9.95		
		0/15		< 1	15	14.95		14.95			14.95		
V_{OL} Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
		10/0		< 1	10		0.05			0.05		0.05	
		15/0		< 1	15		0.05			0.05		0.05	
I_{OH} Output drive drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
		0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
		0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
		0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
	HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
		0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
		0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
		0/15	13.5		15	-4		-3.4	-6.8		-2.8		

a : input on terminals 1, 5, 8, 12 or 2, 6, 9, 13; other inputs to V_{DD}.
b : input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to V_{DD}.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions				Values							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_{OL} Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		
	HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
		0/10	0.5		10	1.5		1.3	2.6		1.1		
		0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_L Input leakage current		0/18	Any input		18		± 0.1		± 10^{-5}	± 0.1		± 1	μA
C_I Input capacitance			Any input						5	7.5			pF

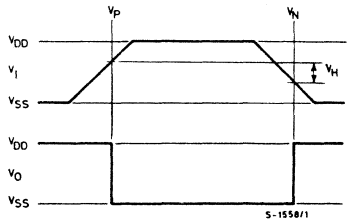
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

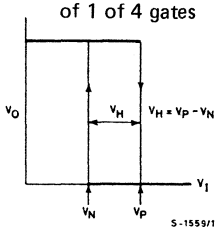
Parameter	Test conditions	Values				Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time		5		300	600	ns
		10		150	300	
		15		120	240	
t_{TLH}, t_{THL} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	

Fig. 1 - Hysteresis definition, characteristic and test setup

(a) Definition of V_P, V_N and V_H



(b) Transfer characteristic of 1 of 4 gates



(c) Test setup

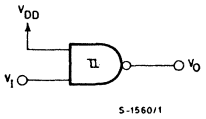


Fig. 2 - Input and output characteristics

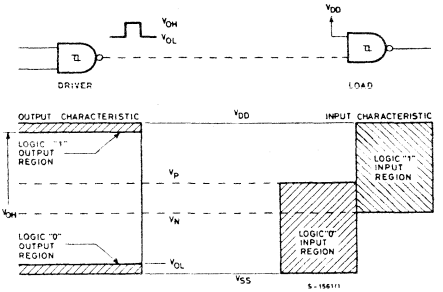


Fig. 3 - Typical current and voltage transfer characteristics

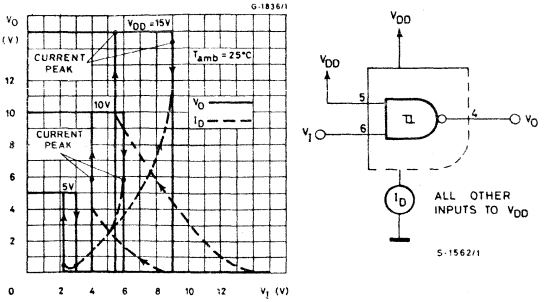


Fig. 4 - Typical voltage transfer characteristics as a function of temperature, and test circuit

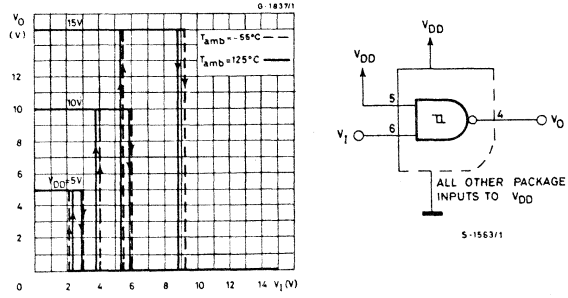


Fig. 5 - Typical output low (sink) current characteristics

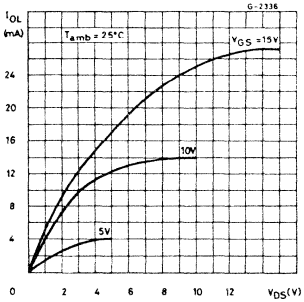


Fig. 6 - Minimum output low (sink) current characteristics

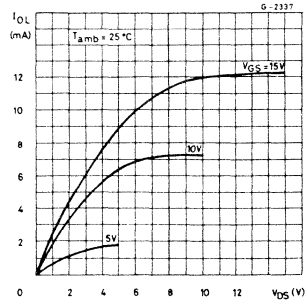


Fig. 7 - Typical output high (source) current characteristics

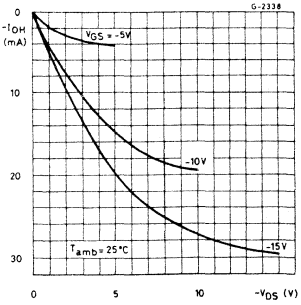


Fig. 8 - Minimum output high (source) current characteristics

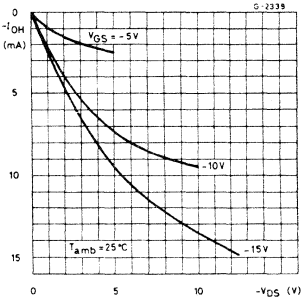


Fig. 9 - Typical propagation delay time vs. supply voltage

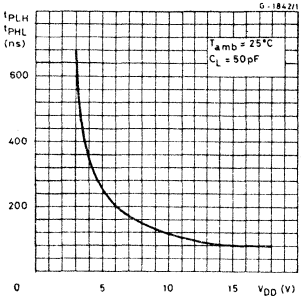


Fig. 10 - Typical transition time vs. load capacitance

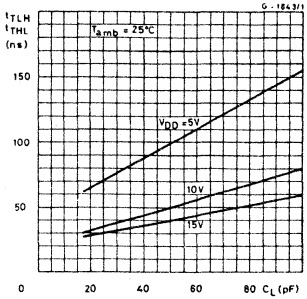


Fig. 11 - Typical trigger threshold voltage vs. V_{DD}

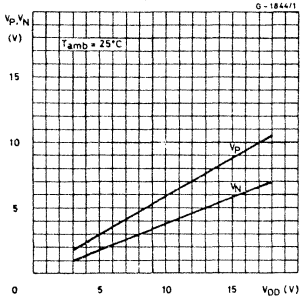


Fig. 12 - Typical per cent hysteresis vs. supply voltage

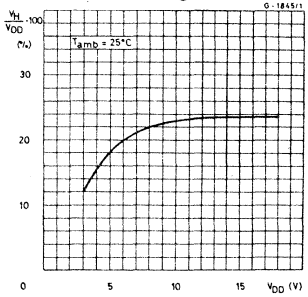


Fig. 13 - Typical dissipation characteristics

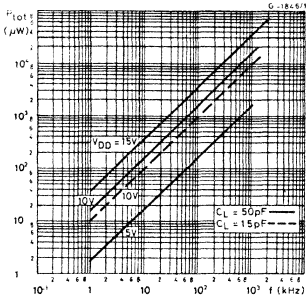
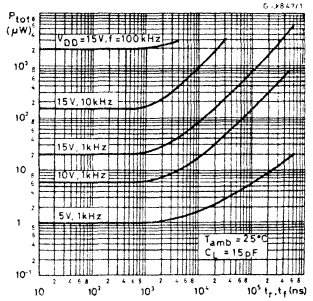


Fig. 14 - Power dissipation vs. rise and fall times



APPLICATIONS

Fig. 15 - Wave shaper

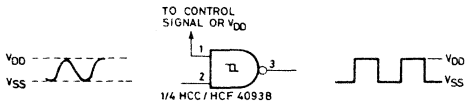
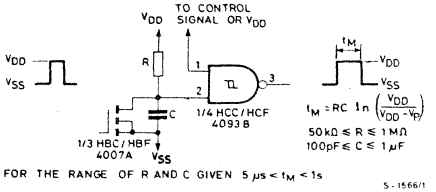
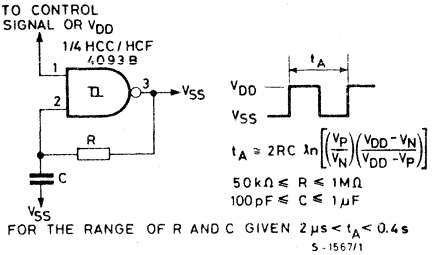


Fig. 16 - Monostable multivibrator



APPLICATIONS (continued)

Fig. 17 - Astable multivibrator



TEST CIRCUITS

Fig. 18 - Quiescent device current

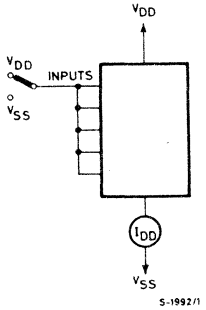
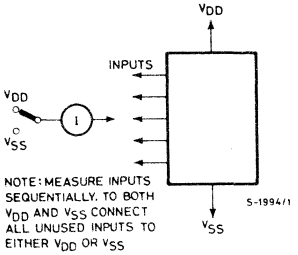


Fig. 19 - Input leakage current



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

8-STAGE SHIFT-AND-STORE BUS REGISTER

- 3-STATE PARALLEL OUTPUTS FOR CONNECTION TO COMMON BUS
- SEPARATE SERIAL OUTPUTS SYNCHRONOUS TO BOTH POSITIVE AND NEGATIVE CLOCK EDGES FOR CASCADING
- MEDIUM SPEED OPERATION - 5 MHz AT 10V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4094B** (extended temperature range) and **HCF 4094B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4094B** is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high. Two serial outputs are available for cascading a number of **HCC/HCF 4094B** devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading **HCC/HCF 4094B** devices when the clock rise time is slow.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

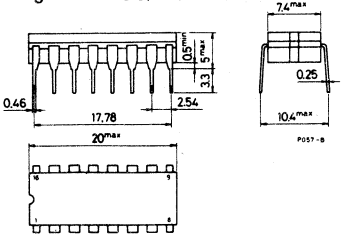
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

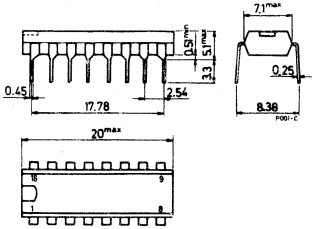
HCC 4094 BD for dual in-line ceramic package
HCC 4094 BF for dual in-line ceramic package, frit seal
HCC 4094 BK for ceramic flat package
HCF 4094 BE for dual in-line plastic package
HCF 4094 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

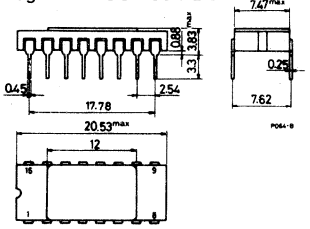
Dual in-line ceramic package for HCC/HCF 4094 BF



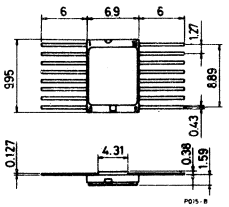
Dual in-line plastic package for HCF 4094 BE



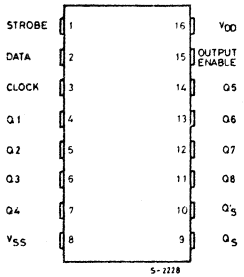
Dual in-line ceramic package for HCC 4094 BD



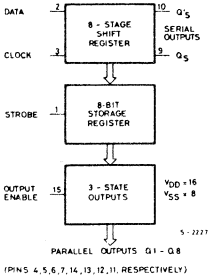
Ceramic flat package for HCC 4094 BK



CONNECTION DIAGRAM



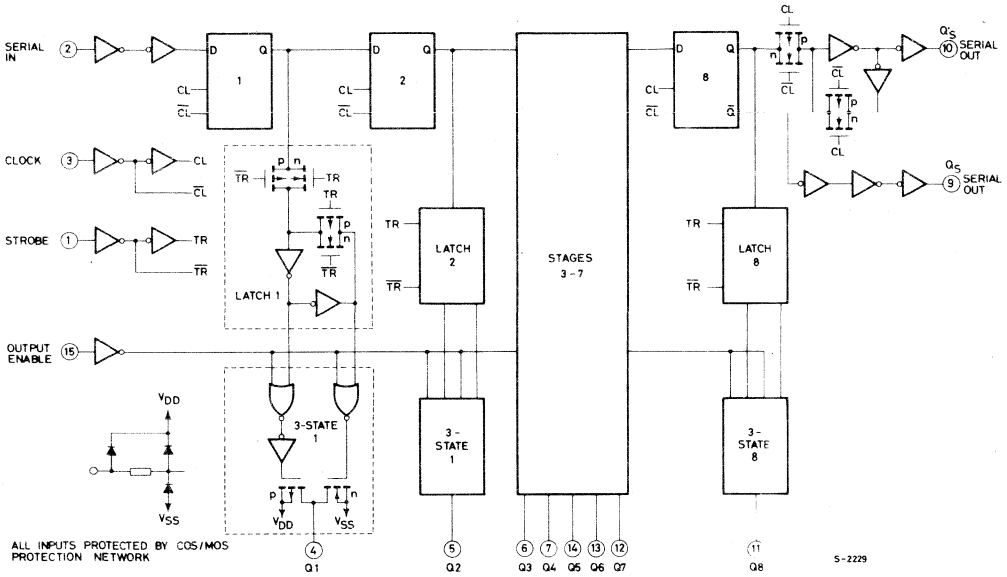
FUNCTIONAL DIAGRAM



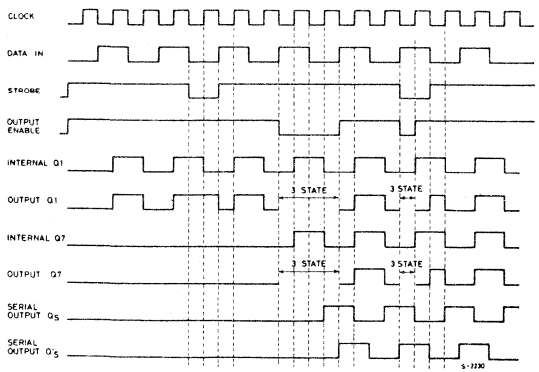
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM



TIMING DIAGRAM



TRUTH TABLE

CL▲	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	QN	QS*	Q'S
⌐	0	X	X	OC	OC	Q7	NC
⌙	0	X	X	OC	OC	NC	Q7
⌐	1	0	X	NC	NC	Q7	NC
⌐	1	1	0	0	Q_{N-1}	Q7	NC
⌐	1	1	1	1	Q_{N-1}	Q7	NC
⌙	1	1	1	NC	NC	NC	Q7

▲ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit
Logic 1 ≡ High
Logic 0 ≡ Low

*At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		$±10^{-5}$	±0.1		± 1	μA
I_{OH},I_{OL}***	3-state output leakage current		0/18	0/18		18		± 0.4		$±10^{-4}$	± 0.4		± 12	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

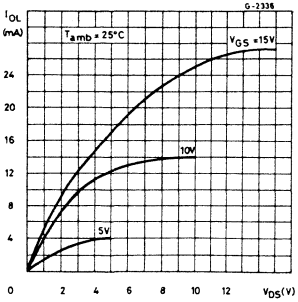
** Any input

*** Forced output disabled

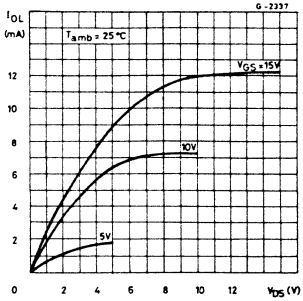
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation dealy time (Clock to serial output Q_S)	5		300	600	ns
		10		125	250	
		15		95	190	
t_{PLH}, t_{PHL}	Propagation delay time (Clock to serial output Q'_S)	5		230	460	ns
		10		110	220	
		15		75	150	
t_{PLH}, t_{PHL}	Propagation delay time (Clock to parallel output)	5		420	840	ns
		10		195	390	
		15		135	270	
t_{PLH}, t_{PHL}	Propagation delay time (Strobe to parallel output)	5		290	580	ns
		10		145	290	
		15		100	200	
t_{PHL}	Propagation delay time (Output enable to parallel output)	5		140	280	ns
		10		75	150	
		15		55	110	
t_{PLH}	Propagation delay time (Output enable to parallel output)	5		225	450	ns
		10		95	190	
		15		70	140	
t_W	Strobe pulse width	5	200	100		ns
		10	80	40		
		15	70	35		
t_W	Clock pulse width	5	200	100		ns
		10	100	50		
		15	83	40		
t_{setup}	Data setup time	5	125	60		ns
		10	55	30		
		15	35	20		
t_{TLH}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_r, t_f	Clock input rise or fall time	5			15	μs
		10			5	
		15			5	
f_{max}	Maximum clock input frequency	5	1.25	2.5		MHz
		10	2.5	5		
		15	3	6		

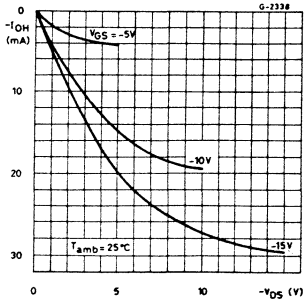
Typical output low (sink) current characteristics



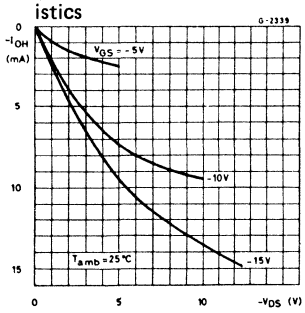
Minimum output low (sink) current characteristics



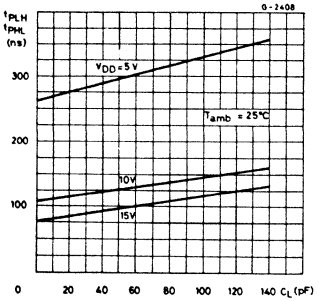
Typical output high (source) current characteristics



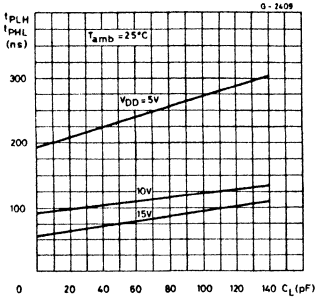
Minimum output high (source) current characteristics



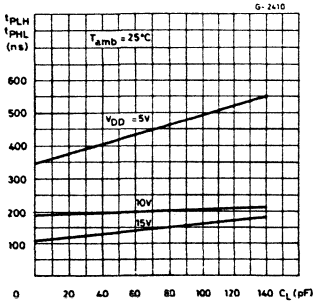
Clock-to-serial output Q_S propagation delay vs. C_L



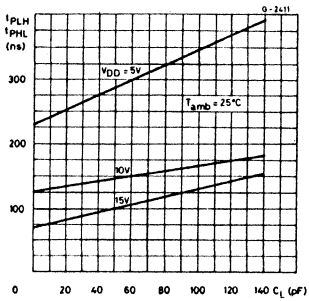
Clock-to-serial output Q'_S propagation delay vs. C_L



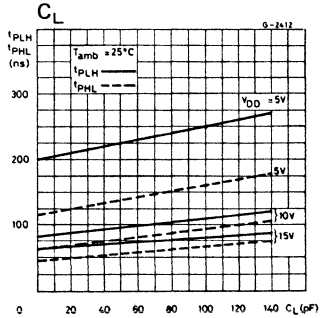
Clock-to-parallel output propagation delay vs. C_L



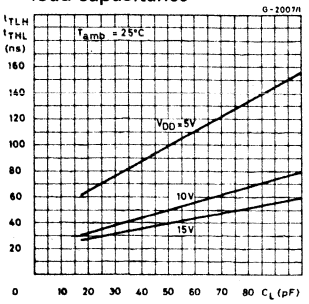
Strobe-to-parallel output propagation delay vs. C_L



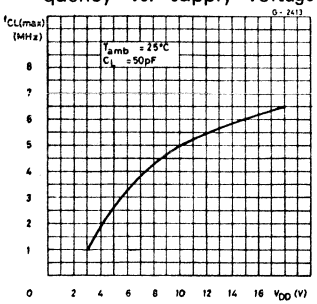
Output enable-to-parallel output propagation delay vs. C_L



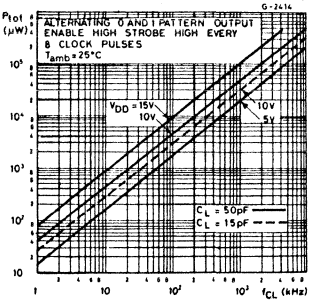
Typical transition time vs. load capacitance



Typical maximum-clock frequency vs. supply voltage

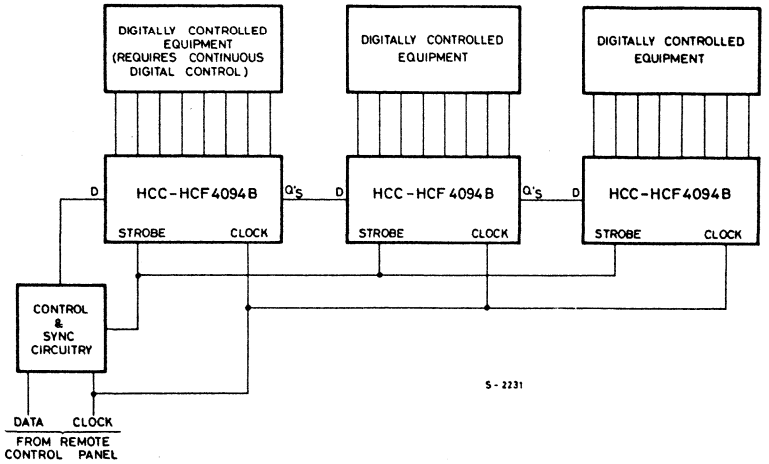


Dynamic power dissipation vs. input clock frequency



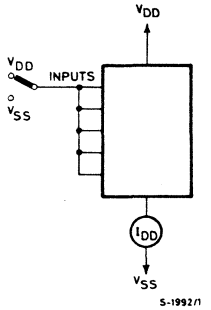
TYPICAL APPLICATION

Remote control holding register

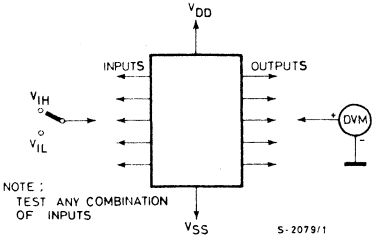


TEST CIRCUITS

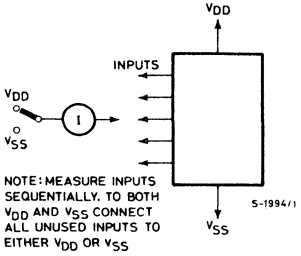
Quiescent device current



Noise immunity



Input leakage current



COS/MOS INTEGRATED CIRCUITS

HCC/HCF 4095B
HCC/HCF 4096B

PRELIMINARY DATA

GATED J-K MASTER-SLAVE FLIP-FLOPS

- 16 MHz TOGGLE RATE (TYP.) AT V_{DD}-V_{SS}= 10V
- GATED INPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4095B/4096B** (extended temperature range) and **HCF 4095B/4096B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package and ceramic flat package.

The **HCC/HCF 4095B** and **HCC/HCF 4096B** are J-K Master-Slave Flip-Flops featuring separate AND gating of multiple J and K inputs. The gated J-K inputs control transfer of information into the master section during clocked operation. Information on the J-K inputs is transferred to the Q and $\overline{Q}$ outputs on the positive edge of the clock pulse. SET and RESET inputs (active high) are provided for asynchronous operation.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

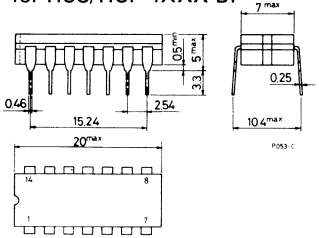
ORDERING NUMBERS:

HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

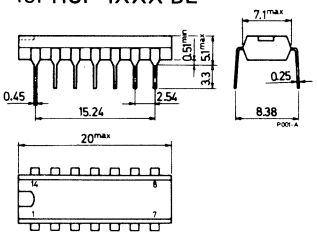
HCC/HCF 4095B
HCC/HCF 4096B

MECHANICAL DATA (dimensions in mm)

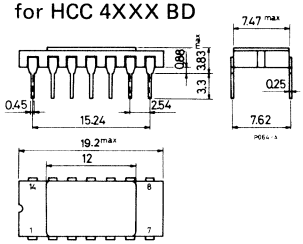
Dual in-line ceramic package
for HCC/HCF 4XXX BF



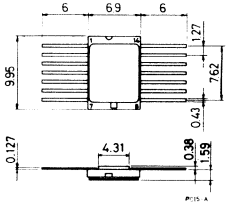
Dual in-line plastic package
for HCF 4XXX BE



Dual in-line ceramic package
for HCC 4XXX BD

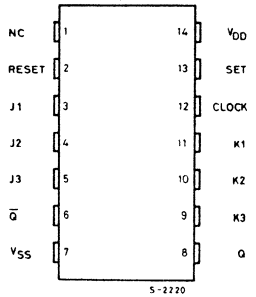


Ceramic flat package
for HCC 4XXX BK

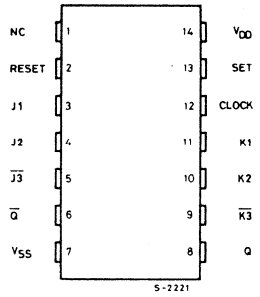


CONNECTION DIAGRAMS

For **4095B**



For **4096B**

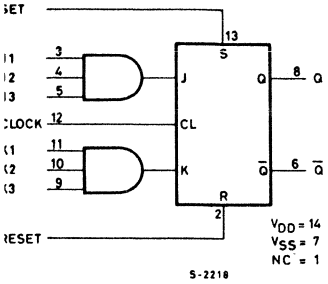


RECOMMENDED OPERATING CONDITIONS

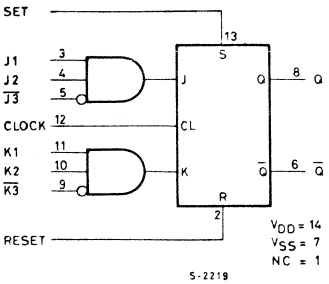
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

FUNCTIONAL DIAGRAMS

For **4095B**

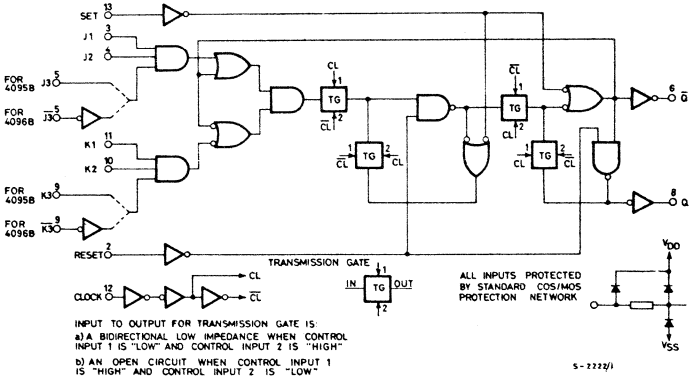


For **4096B**



LOGIC DIAGRAM

For **4095B** and **4096B**



TRUTH TABLES

SYNCHRONOUS OPERATION (S=0 R=0)

Inputs Before Positive Clock Transition		Outputs After Positive Clock Transition	
J*	K*	Q	$\overline{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	Toggles	

* For **4095B**
J = J1 · J2 · J3
K = K1 · K2 · K3

For **4096B**
J = J1 · J2 · $\overline{J3}$
K = K1 · K2 · $\overline{K3}$

ASYNCHRONOUS OPERATION (J and K - DON'T CARE)

S	R	Q	$\overline{Q}$
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	0	0

0 = V_{SS}, 1 = V_{DD}

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

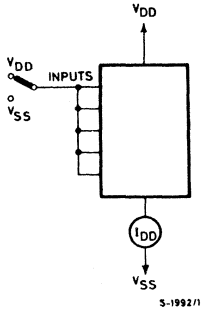
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

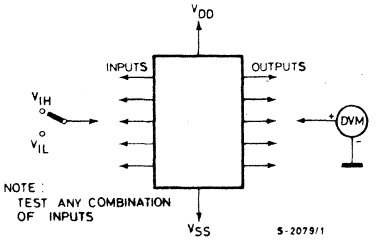
Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time	5		250	500	ns
		10		100	200	
		15		75	150	
t_{PLH}, t_{PHL}	Propagation delay time (Set or reset)	5		150	300	ns
		10		75	150	
		15		50	100	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}	Maximum clock input frequency	5	3.5	7		MHz
		10	8	16		
		15	12	24		
t_W	Clock pulse width	5	140	70		ns
		10	60	30		
		15	40	20		
t_r, t_f	Clock input rise or fall time	5			15	μs
		10			5	
		15			5	
t_W	Set or reset pulse width	5	200	100		ns
		10	100	50		
		15	50	25		
t_{setup}	Data setup time	5	400	200		ns
		10	160	80		
		15	100	50		

TEST CIRCUITS

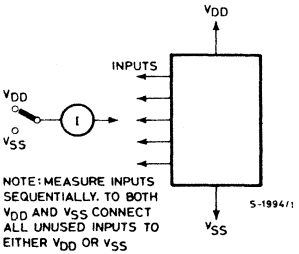
Quiescent device current



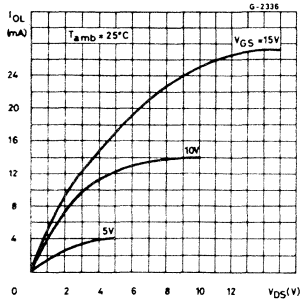
Input voltage



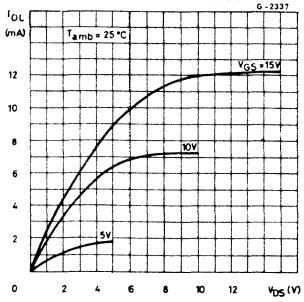
Input leakage current



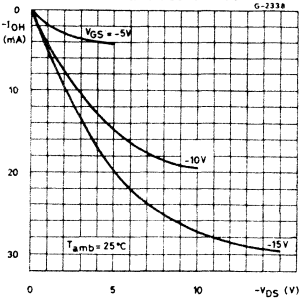
Typical output low (sink) current characteristics



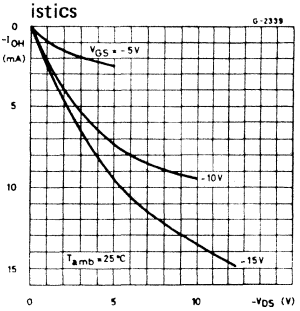
Minimum output low (sink) current characteristics



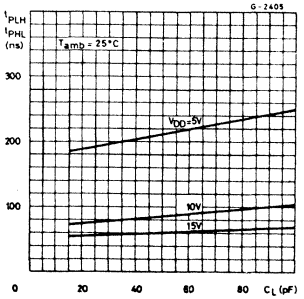
Typical output high (source) current characteristics



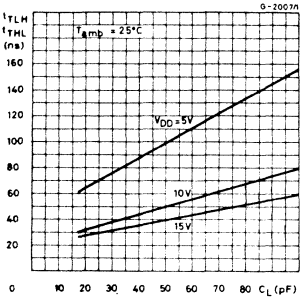
Minimum output high (source) current characteristics



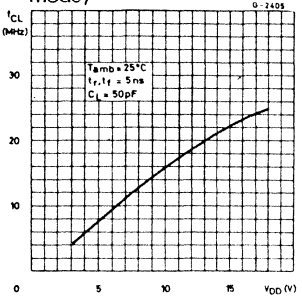
Typical propagation delay time vs. load capacitance



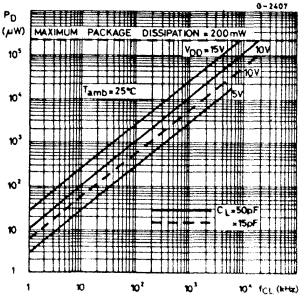
Typical transition time vs. load capacitance



Typical clock frequency vs. supply voltage (toggle mode)

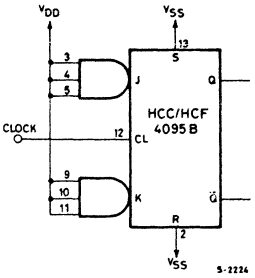


Typical power dissipation vs. input clock frequency

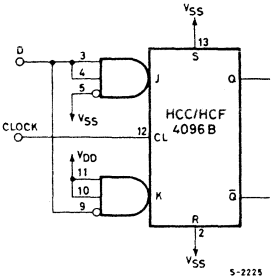


TYPICAL APPLICATIONS

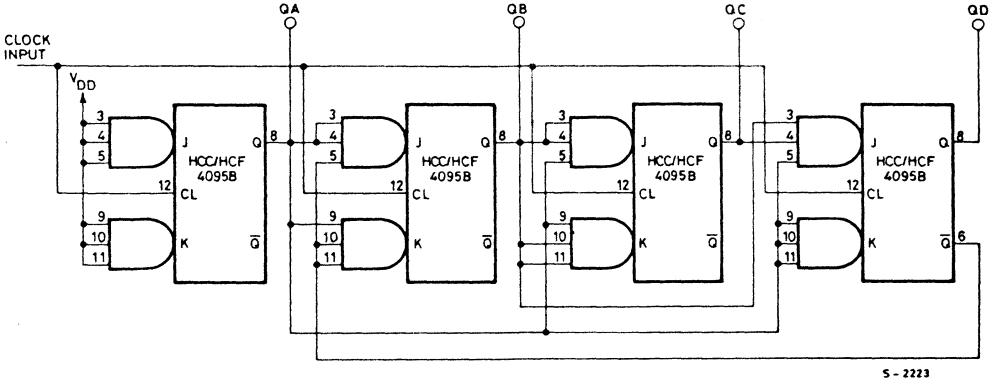
T-type flip-flop

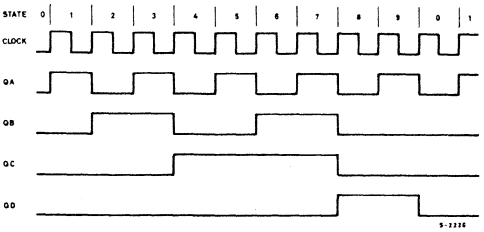


D-type flip-flop



Synchronous binary divide-by-ten counter



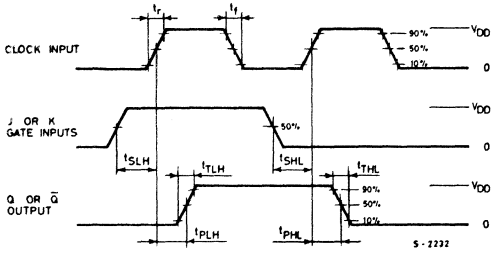


STATE	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

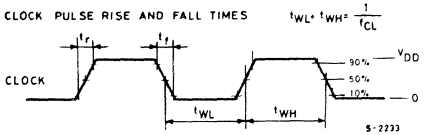
NOTE:
In all 4095B units the set and Reset are connected to V_{SS}

WAVEFORMS

Propagation delay, transition and setup-time



Clock pulse rise and fall time



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

DUAL MONOSTABLE MULTIVIBRATOR

- RETRIGGERABLE/RESETTABLE CAPABILITY
- TRIGGER AND RESET PROPAGATION DELAYS INDEPENDENT OF R_X, C_X
- TRIGGERING FROM LEADING OR TRAILING EDGE
- Q AND $\overline{Q}$ BUFFERED OUTPUTS AVAILABLE
- SEPARATE RESETS
- WIDE RANGE OF OUTPUT-PULSE WIDTHS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4098B** (extended temperature range) and **HCF 4098B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4098B** dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application. An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X. Leading-edge-triggering (+ TR) and trailing-edge-triggering (- TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused -TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the **4098B** is not used, its RESET should be tied to V_{SS}. See Table I. In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-triggerable mode, $\overline{Q}$ is connected to -TR when leading-edge triggering (+ TR) is used or Q is connected to +TR when trailing-edge triggering (- TR) is used. The time period (T) for this multivibrator can be approximated by: $T_X = \frac{1}{2} R_X C_X$ for $C_X \geqslant 0.01\ \mu F$. Time periods as a function of R_X for values of C_X and V_{DD} are given in Fig. 8. Values of T vary from unit to unit and as a function of voltage, temperature, and $R_X C_X$. The minimum value of external resistance, R_X, is 5 kΩ. The maximum value of external capacitance, C_X, is 100 μF. Fig. 9 shows time periods as a function of C_X for values of R_X and V_{DD}. The output pulse width has variations of ± 2.5% typically, over the temperature range of -55°C to 125°C for C_X = 1000 pF and R_X = 100 kΩ. For power supply variations of ± 5%, the output pulse width has variations of ± 0.5% typically, for V_{DD} = 10V and 15V and ± 1% typically, for V_{DD} = 5V at C_X = 1000 pF and R_X = 5 kΩ.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

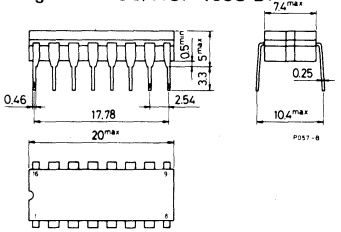
HCC/HCF 4098B

ORDERING NUMBERS:

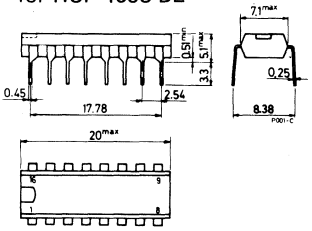
HCC 4098 BD for dual in-line ceramic package
HCC 4098 BF for dual in-line ceramic package, frit seal
HCC 4098 BK for ceramic flat package
HCF 4098 BE for dual in-line plastic package
HCF 4098 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

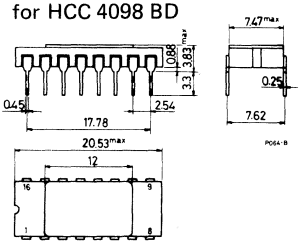
Dual in-line ceramic package for HCC/HCF 4098 BF



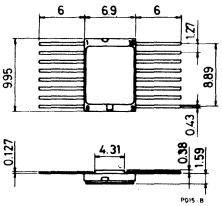
Dual in-line plastic package for HCF 4098 BE



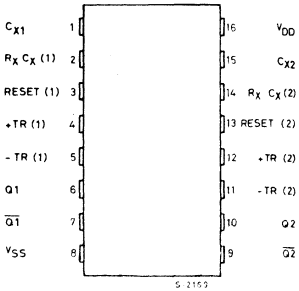
Dual in-line ceramic package for HCC 4098 BD



Ceramic flat package for HCC 4098 BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

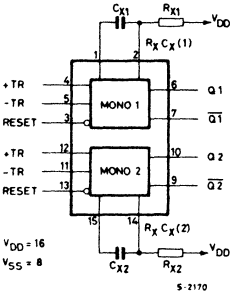


Fig. 1 - Logic diagram

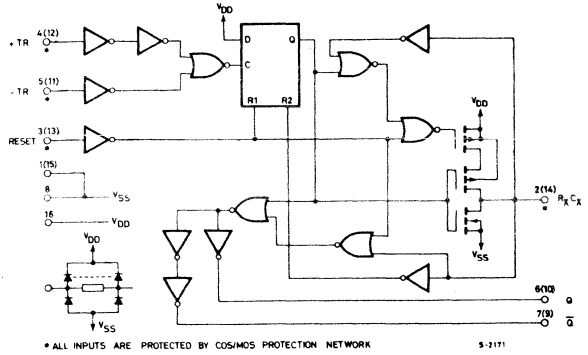
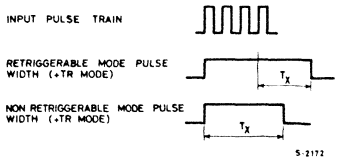


TABLE 1 - Functional terminal connections

FUNCTION	TERMINAL CONNECTIONS						OTHER CONNECTIONS	
	TO V_{DD}		TO V_{SS}		INPUT PULSE TO			
	Mono(1)	Mono(2)	Mono(1)	Mono(2)	Mono(1)	Mono(2)	Mono(1)	Mono(2)
Leading - Edge Trigger/Retriggerable	3, 5	11, 13			4	12		
Leading - Edge Trigger/Non-retriggerable	3	13			4	12	5, 7	11, 9
Trailing - Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing - Edge Trigger/Non-retriggerable	3	13			5	11	4, 6	12, 10
Unused Section	5	11	3, 4	12, 13				

NOTES: 1) A Refriggerable one-shot multivibrator has an output pulse width which is extended one full time period (T_X) after application of the last trigger pulse.
2) A Non-retriggerable one-shot multivibrator has a time period T_X referenced from the application of the first trigger pulse.



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				1.5/13.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}	Input leakage current		0/18	Any input		18		±0.1		±10^{-5}	±0.1		±1	μA
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions			Values			Unit
		R_X (kΩ)	C_X (pF)	V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Trigger propagation delay time (+TR, -TR to Q, $\bar{Q}$)	5 to 10.000	⩾ 15	5		250	500	ns
				10		125	250	
				15		100	200	
t_{WH}, t_{WL}	Trigger pulse width	5 to 10.000	⩾ 15	5	140	70		ns
				10	60	30		
				15	40	20		
t_{TLH}	Transition time	5 to 10.000	⩾ 15	5		100	200	ns
				10		50	100	
				15		40	80	
t_{THL}	Transition time	5 to 10.000	15 to 10.000	5		100	200	
				10		50	100	
				15		40	80	
		5 to 10.000	0,01 μF to 0,1 μF	5		150	300	
				10		75	150	
				15		65	130	
		5 to 10.000	0.1 μF to 1 μF	5		250	500	
				10		150	300	
				15		80	160	
t_{PLH}, t_{PHL}	Propagation,delay time (Reset)	5 to 10.000	⩾ 15	5		225	450	ns
				10		125	250	
				15		75	150	
t_WR	Pulse width (Reset)	100	15	5	200	100		ns
				10	80	40		
				15	60	30		
			1000	5	1200	600		
				10	600	300		
				15	500	250		
			0.1 μF	5	50	25		μs
				10	30	15		
				15	20	10		
t_r, t_f(TR)	Rise or fall time (Trigger)		5 to 15				100	μs
	Pulse width match between circuits in same package	10	10.000	5		5	10	%
				10		7.5	15	
				15		7.5	15	

Fig. 2 - Typical output low (sink) current characteristics

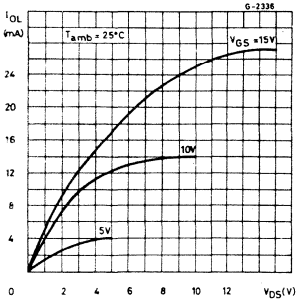


Fig. 3 - Minimum output low (sink) current characteristics

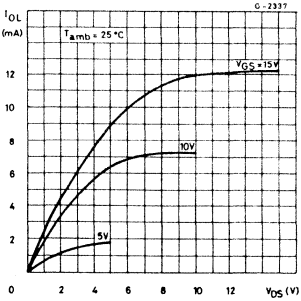


Fig. 4 - Typical output high (source) current characteristics

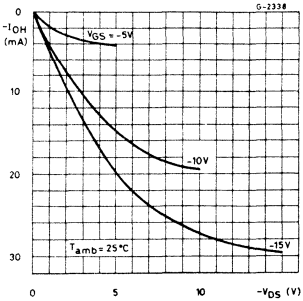


Fig. 5 - Minimum output high (source) current characteristics

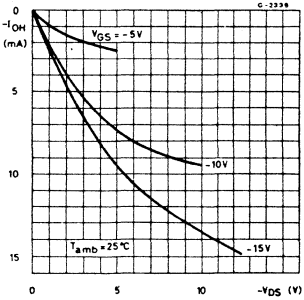


Fig. 6 - Typical propagation delay time vs. load capacitance, trigger in to Q out. (All values of C_X and R_X)

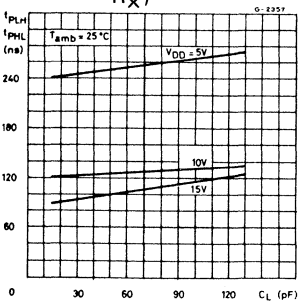


Fig. 7 - Transition time vs. load capacitance for $R_X = 5\ k\Omega$, 10000 $k\Omega$ and $C_X = 15$ pF, 10000 pF

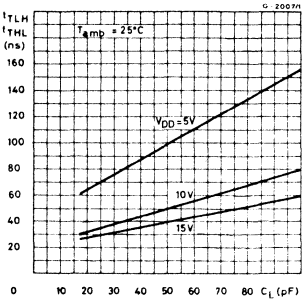


Fig. 8 - Typical external resistance vs. pulse width at various V_{DD} and C_X

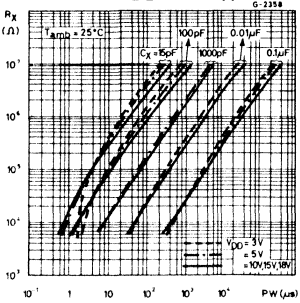


Fig. 9 - Typical external capacitance vs. pulse width at various V_{DD} and R_X

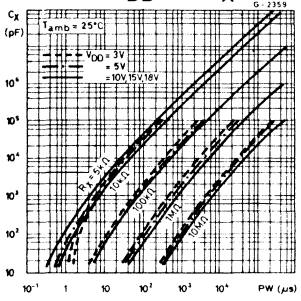


Fig. 10 - Typical minimum reset pulse width vs. external capacitance

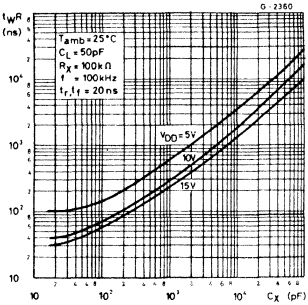
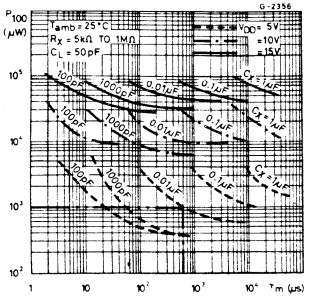
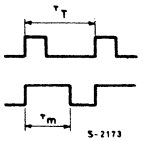


Fig. 11 - Average power dissipation for 100% duty cycle vs. one-shot pulse width



To calculate average power dissipation (P) for less than 100% duty cycle:
P_{100}= average power for 100% duty cycle
$P = (\frac{\tau_m}{\tau_T}) P_{100}$ where τ_m = one-shot pulse width
τ_T = trigger pulse period
e.g.: For τ_m = 600 μs τ_T = 1000 μs, C_X = 0.01 μF, V_{DD} = 5V
$P = (\frac{600}{1000})\ 10^3$ μW = 600 μW (see dotted line on graph)



TEST CIRCUITS

Fig. 12 - Quiescent - device current

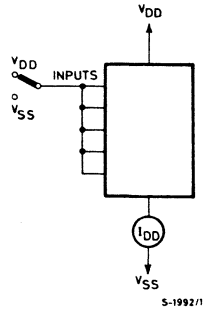


Fig. 13 - Input - voltage

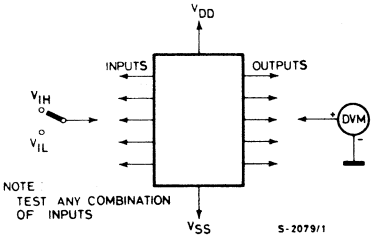
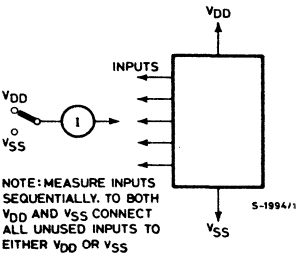
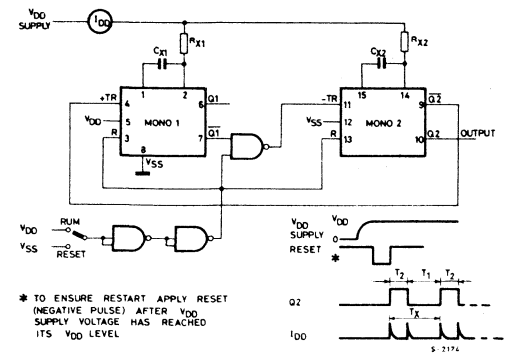


Fig. 14 - Input leakage



APPLICATIONS

Fig. 15 - Astable multivibrator with restart after reset capability

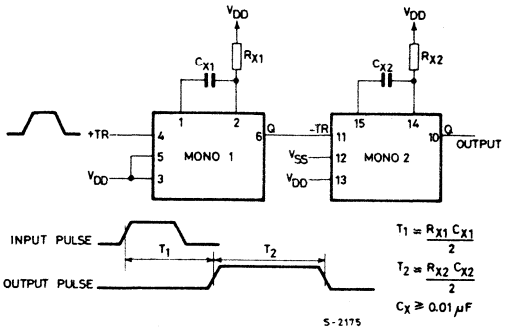


R_X	I_{DD} (Avg)	T_X (T1+T2)	V_{DD}
10 kΩ	1 mA ↓ 0.05 mA	3.8 μs ↓ 0.5 s	5V
	2.5 mA ↓ 0.5 mA	3.2 μs ↓ 0.5 s	10V
10 MΩ	5 mA ↓ 1 mA	3 μs ↓ 0.5 s	15V

Notes: All values are typical.
C_X range: 0.0001 μF to 0.1 μF.

APPLICATIONS (continued)

Fig. 16 - Pulse delay



COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4099B

PRELIMINARY DATA

8-BIT ADDRESSABLE LATCH

- SERIAL DATA INPUT - ACTIVE PARALLEL OUTPUT
- STORAGE REGISTER CAPABILITY - MASTER CLEAR
- CAN FUNCTION AS DEMULTIPLEXER
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4099B** (extended temperature range) and **HCF 4099B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4099B** 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions. Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs. A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

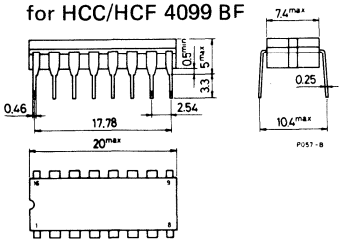
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

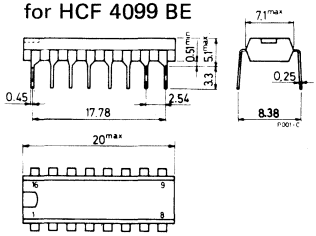
HCC 4099 BD for dual in-line ceramic package
HCC 4099 BF for dual in-line ceramic package, frit seal
HCC 4099 BK for ceramic flat package
HCF 4099 BE for dual in-line plastic package
HCF 4099 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

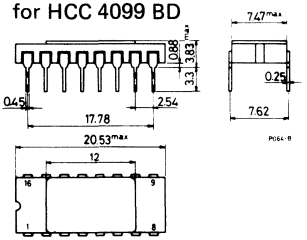
Dual in-line ceramic package for HCC/HCF 4099 BF



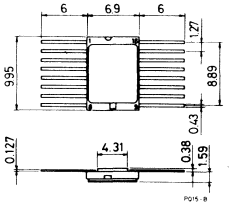
Dual in-line plastic package for HCF 4099 BE



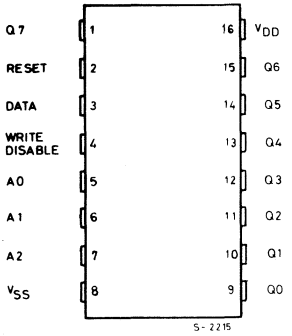
Dual in-line ceramic package for HCC 4099 BD



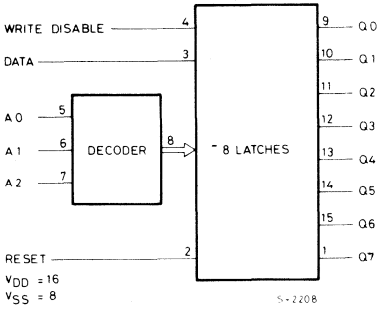
Ceramic flat package for HCC 4099 BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

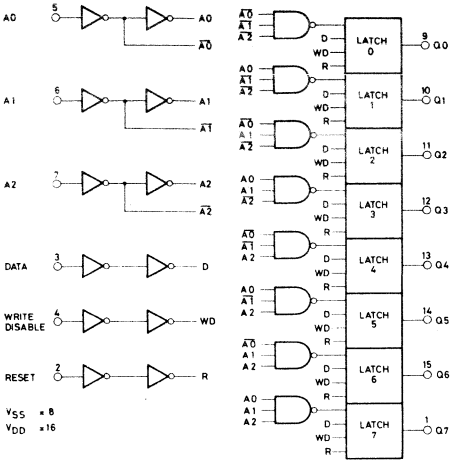


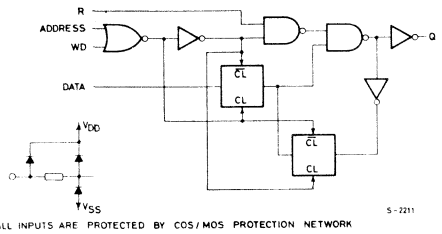
RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage		3 to 18	V
V_I	Input voltage		0 to V_{DD}	V
T_{op}	Operating temperature:	for **HCC** types	-55 to 125	°C
		for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM

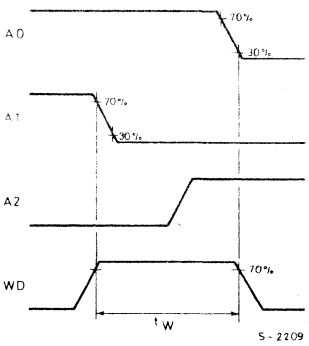
1 of 8 latches





ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

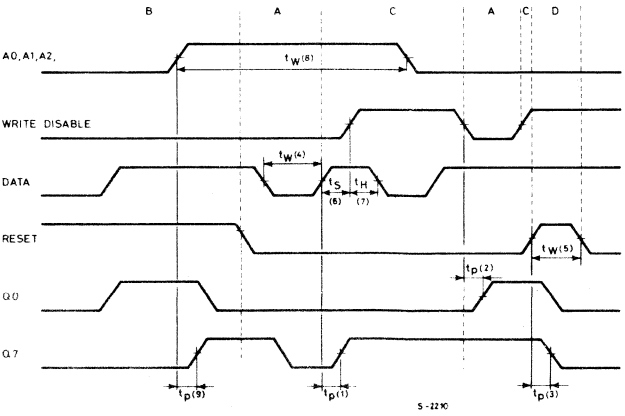
Definition of WRITE DISABLE ON time



TYPES	MODE SELECTION			
	WD	R	ADDRESSED LATCH	UNADDRESSED LATCH
A	0	0	Follows Data	Holds Previous State
B	0	1	Follows Data (Active High 8-Channel Demultiplexer)	Reset to "0"
C	1	0	Holds Previous State	
D	1	1	Reset to "0"	Reset to "0"

WD = WRITE DISABLE R = RESET

Master timing diagram



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

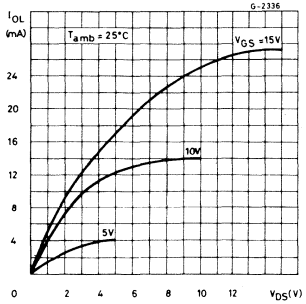
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

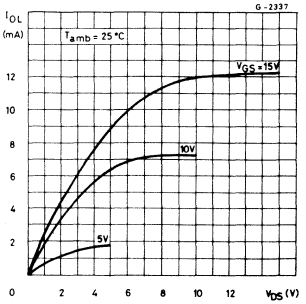
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter			Test conditions (see master timing diagram)	V_{DD}(V)	Values Min.	Typ.	Max.	Unit
t_{PLH}, t_{PHL}	Propagation delay time	Data to output	(1)	5		200	400	ns
				10		75	150	
				15		50	100	
		Write disable to output	(2)	5		200	400	
				10		80	160	
				15		60	120	
		Address to output	(9)	5		225	450	
				10		100	200	
				15		75	150	
t_{PHL}	Propagation delay time	Reset to output	(3)	5		175	350	
				10		80	160	
				15		65	130	
t_{THL}, t_{TLH}	Transition time	Any output		5		100	200	ns
				10		50	100	
				15		40	80	
t_W	Pulse width	Data	(4)	5	200	100		ns
				10	100	50		
				15	80	40		
		Address	(8)	5	400	200		
				10	200	100		
				15	125	65		
		Reset	(5)	5	150	75		
				10	75	40		
				15	50	25		
t_{setup}	Setup time	Data to write disable	(6)	5	100	50		ns
				10	50	25		
				15	35	20		
t_{hold}	Hold time	Data to write disable	(7)	5	150	75		ns
				10	75	40		
				15	50	25		

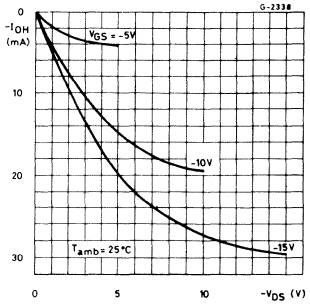
Typical output low (sink) current characteristics



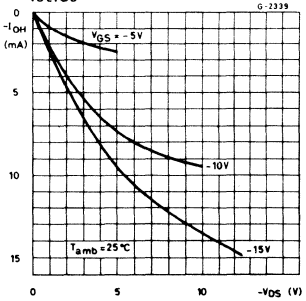
Minimum output low (sink) current characteristics



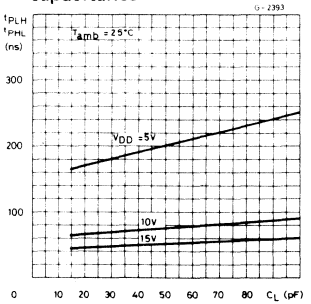
Typical output high (source) current characteristics



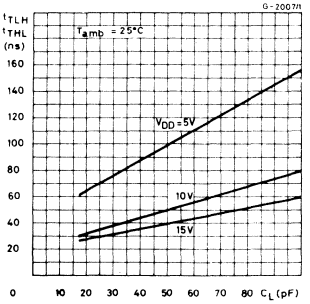
Minimum output high (source) current characteristics



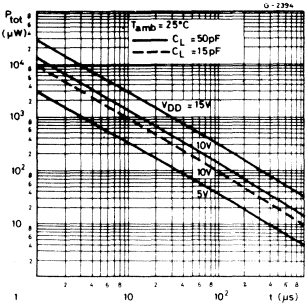
Typical propagation delay time (data to Qn) vs. load capacitance



Typical transition time vs. load capacitance

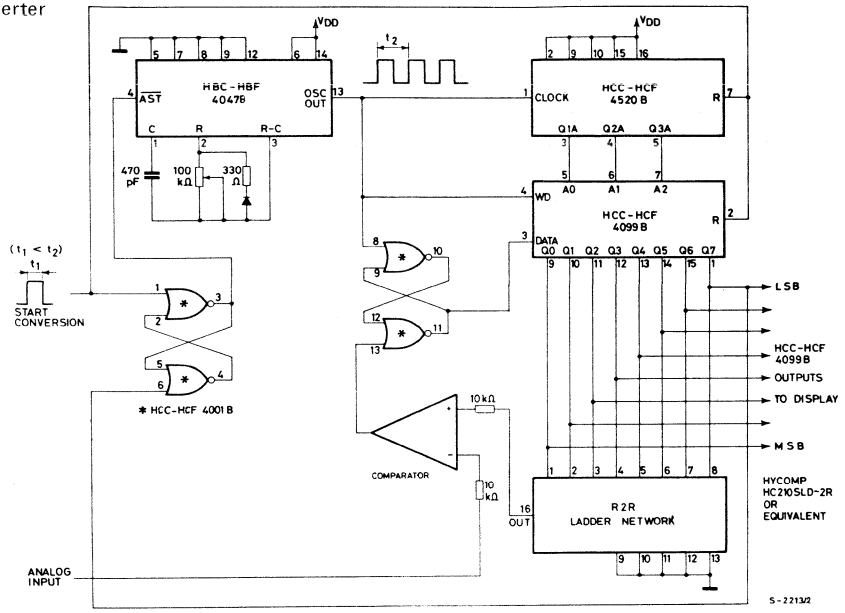


Typical dynamic power dissipation vs. address cycle time

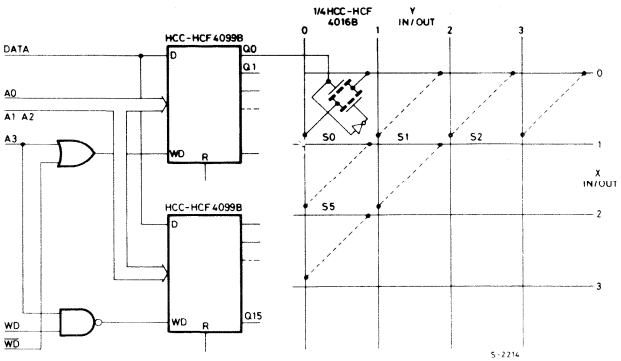


TYPICAL APPLICATIONS

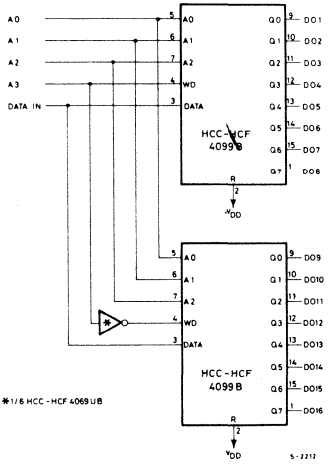
A/D converter



Multiple selection decoding - 4x4 crosspoint switch

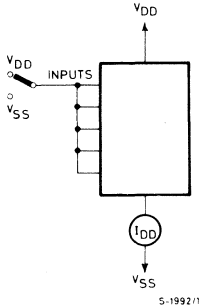


1 of 16 decoder/demultiplexer

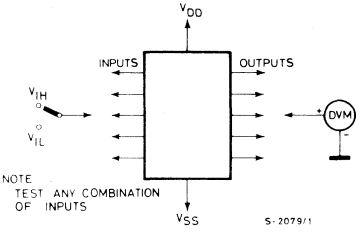


TEST CIRCUITS

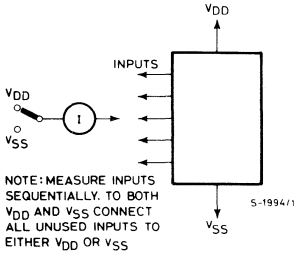
Quiescent device current



Input voltage



Input current



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

STROBED HEX INVERTER/BUFFER

- 2 TTL-LOAD OUTPUT DRIVE CAPABILITY
- 3-STATE OUTPUTS
- COMMON OUTPUT-DISABLE CONTROL
- INHIBIT CONTROL
- 100% TESTED FOR QUIESCENT CURRENT AT 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V OVER FULL PACKAGE-TEMPERATURE RANGE, 100 nA AT 18V AND 25°C
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4502B** (extended temperature range) and **HCF 4502B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4502B** consists of six inverter-buffers with 3-state outputs. A logic "1" on the OUTPUT DISABLE input produces a high-impedance state in all six outputs. This feature permits common busing of the outputs, thus simplifying system design. A logic "1" on the INHIBIT input switches all six outputs to logic "0" if the OUTPUT DISABLE input is a logic "0". This device is capable of driving two standard TTL loads, which is equivalent to six times the JEDEC "B" series I_{OL} standard.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

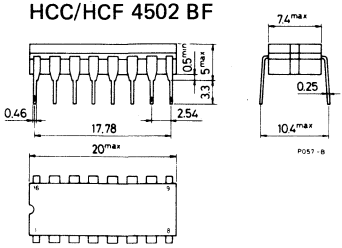
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

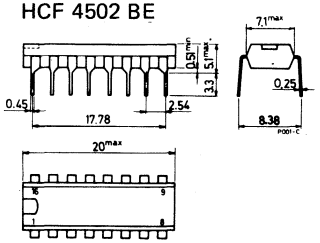
HCC 4502 BD for dual in-line ceramic package
HCC 4502 BF for dual in-line ceramic package, frit seal
HCC 4502 BK for ceramic flat package
HCF 4502 BE for dual in-line plastic package
HCF 4502 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

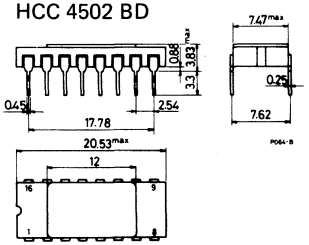
Dual in-line ceramic package for HCC/HCF 4502 BF



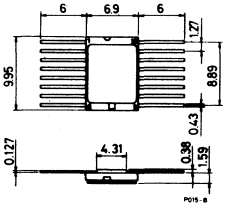
Dual in-line plastic package for HCF 4502 BE



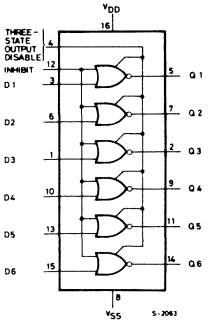
Dual in-line ceramic package for HCC 4502 BD



Ceramic flat package for HCC 4502 BK



CONNECTION DIAGRAM



TRUTH TABLE

DISABLE	INHIBIT	Dn	Qn
0	0	0	1
0	0	I	0
0	I	X	0
I	X	X	Z

X = Don't Care
Z = High Impedance
Logic 1 = High
Logic 0 = Low

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18 V
V_I	Input voltage	0 to V_{DD} V
T_{op}	Operating temperature: for **HCC** types	-55 to 125 °C
	for **HCF** types	-40 to 85 °C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	3.84		3.06	6		0.36		mA
			0/10	0.5		10	9.6		7.8	15.6		5.4		
			0/15	1.5		15	25.2		20.4	40.8		14.4		
		HCF types	0/ 5	0.4		5	3.66		3.06	6		2.52		
			0/10	0.5		10	9		7.8	15.6		6.6		
			0/15	1.5		15	24		20.4	40.8		16.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		$±10^{-5}$	±0.1		± 1	μA
I_{OH},I_{OL}	3-state output leakage current			0/18		18		±2		$±10^{-4}$	± 0.4		±12	μA
C_I**	Input capacitance									5	7.5			pF

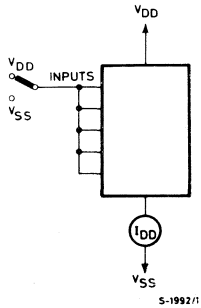
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}	Data or inhibit delay time		5		135	270	ns
			10		60	120	
			15		40	80	
t_{PLH}	Data or inhibit delay time		5		190	380	ns
			10		90	180	
			15		65	30	
t_{PHZ}	Disable delay time (output high to high impedance)		5		60	120	ns
			10		40	80	
			15		30	60	
t_{PZH}	Disable delay time (high impedance to output high)		5		110	220	ns
			10		50	100	
			15		40	80	
t_{PLZ}	Disable delay time (output low to high impedance)		5		125	250	ns
			10		65	130	
			15		55	110	
t_{PZL}	Disable delay time (high impedance to output low)		5		125	250	ns
			10		55	110	
			15		40	80	
t_{TLH}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
t_{THL}	Transition time		5		60	120	ns
			10		30	60	
			15		20	40	

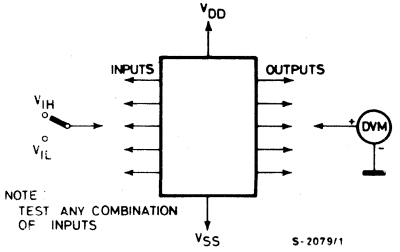
TEST CIRCUIT

Quiescent device current



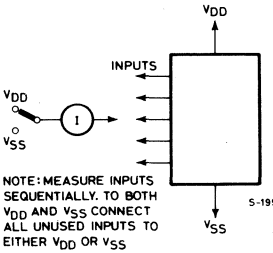
S-1992/1

Input voltage



S-2079/1

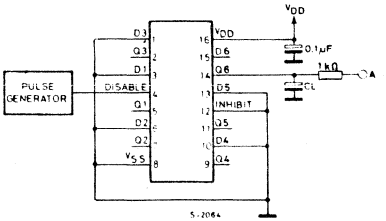
Input leakage current

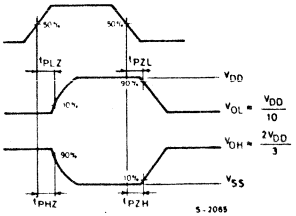


S-1994

Test circuit and waveforms

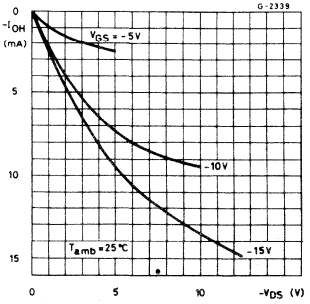
disable delay time



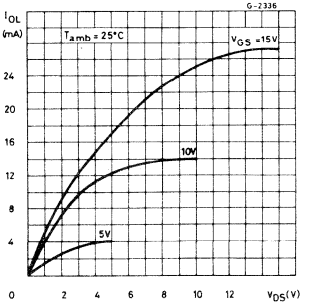


TEST CONDITION		
Test	Pin 15	Point A
t_{PHZ}	V_{SS}	V_{SS}
t_{PLZ}	V_{DD}	V_{DD}
t_{PZL}	V_{DD}	V_{DD}
t_{PZH}	V_{SS}	V_{SS}

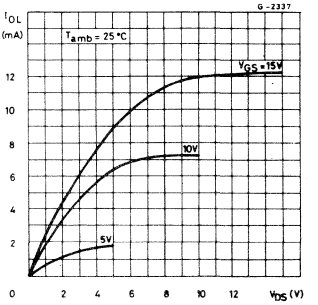
Minimum output high(source) current characteristics



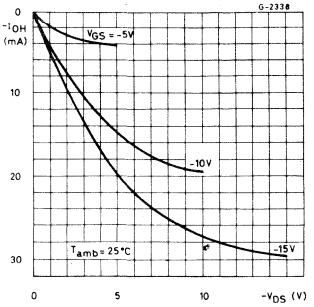
Typical output low (sink) current



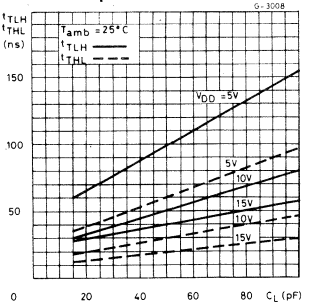
Minimum output low (sink) current characteristics



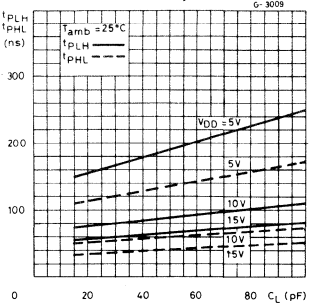
Typical output high (source) current characteristics



Typical transition time vs. load capacitance



Typical propagation delay time vs. load capacitance



COS/MOS INTEGRATED CIRCUIT

HCC/HCF 4508B

PRELIMINARY DATA

DUAL 4-BIT LATCH

- TWO INDIPENDENT 4-BIT LATCHES
- INDIVIDUAL MASTER RESET FOR EACH 4-BIT-LATCH
- 3-STATE OUTPUTS WITH HIGH-IMPEDANCE STATE FOR BUS LINE APPLICATION
- MEDIUM-SPEED OPERATION: $t_{PHL} = t_{PLH} = 70$ ns (TYP.) AT $V_{DD} = 10V$ AND $C_L = 50$ pF
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS

The **HCC 4508B** (extended temperature range) and the **HCF 4508B** (intermediate temperature range) are monolithic integrated circuits available in 24-lead dual in-line plastic and ceramic slam package. The **HCC/HCF 4508B** dual 4-bit latch contains two identical 4-bit latches with separate STROBE, RESET, and OUTPUT DISABLE controls. With the STROBE line in the high state, the data on the "D" inputs appear at the corresponding "Q" outputs provided the DISABLE line is in the low state. Changing the STROBE line to the low state locks the data into the latch. A high on the reset line forces the outputs to a low level regardless of the state of the STROBE input. The outputs are forced to the high-impedance state for bus line applications by a high level on the DISABLE input.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

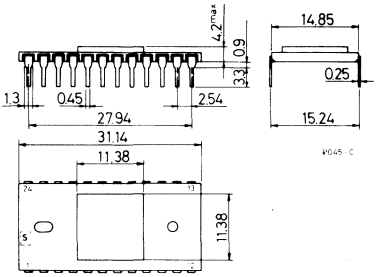
ORDERING NUMBERS:

HCC 4508 BD for dual in-line ceramic slam package
HCF 4508 BD for dual in-line ceramic slam package
HCF 4508 BE for dual in-line plastic package

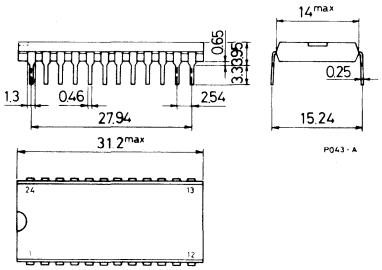
HCC/HCF 4508 B

MECHANICAL DATA (dimensions in mm)

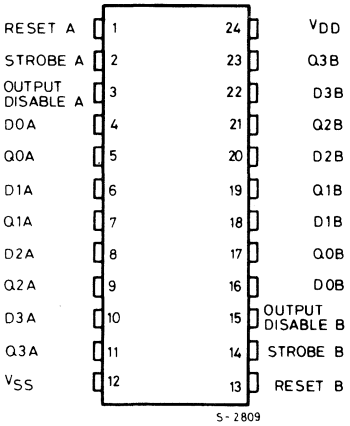
Dual in-line ceramic slam package
for HCC/HCF 4508B



Dual in-line plastic package
for HCF 4508B

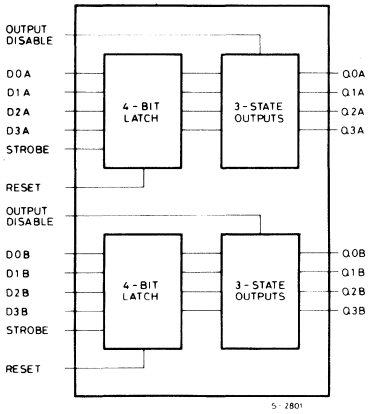


CONNECTION DIAGRAM



S-2809

FUNCTIONAL DIAGRAM



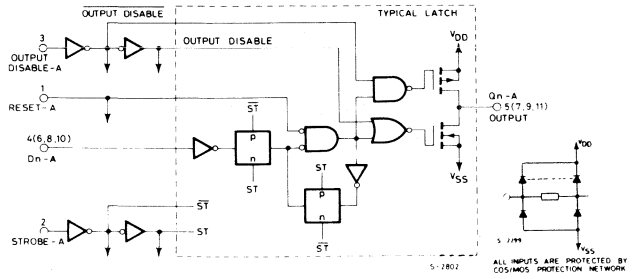
S-2801

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_i	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM (A Section)

1 of 4 identical latches with common output disable, reset and strobe



TRUTH TABLE

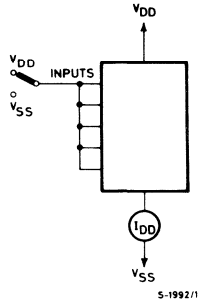
RESET	DISAB.	STROBE	D INPUT	Q INPUT
0	0	1	1	1
0	0	1	0	0
0	0	0	X	Latched
1	0	X	X	0
X	1	X	X	Z

1 = High level
0 = Low level

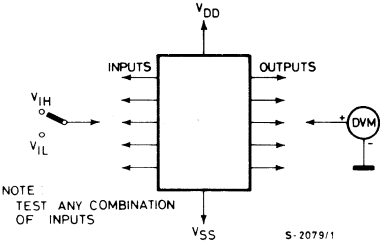
X = Dont' care
Z = High impedance

TEST CIRCUITS

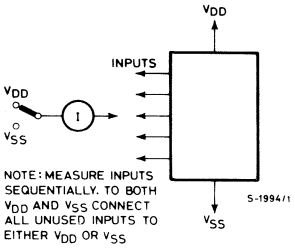
Quiescent device current test circuit



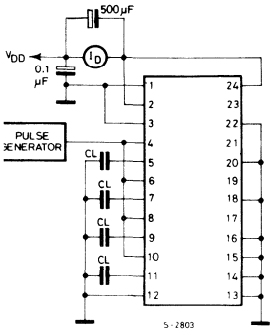
Input voltage test circuit



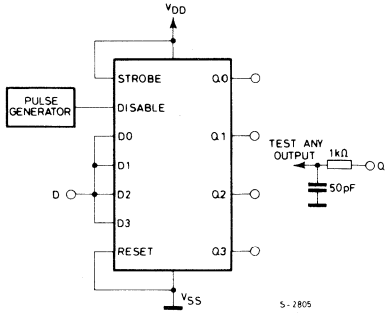
Input current test circuit



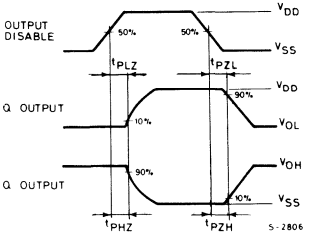
Power dissipation test circuit



Output disable



Waveform



CHAR.	TEST. AT D	VOLT. AT Q
t_{PHZ}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}
t_{PZH}	V_{DD}	V_{SS}

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

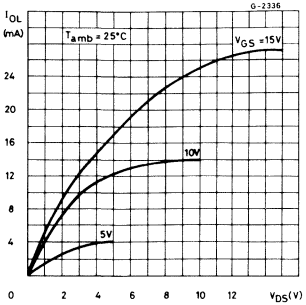
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
I_O	3-state output leakage current		0/18	0/18		0/18		± 0.4		$\pm 10^{-4}$			± 0.4	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

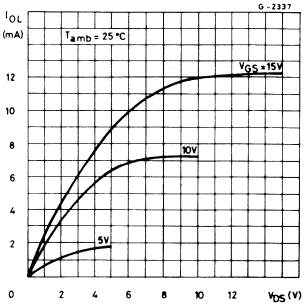
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ, unless otherwise specified)

Parameter			Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{THL}, t_{TLH}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
$t_{W(R)}$	Reset pulse width		5	200	100		ns
			10	140	70		
			15	100	50		
$t_{W(st)}$	Strobe pulse width		5	140	70		ns
			10	80	40		
			15	70	35		
t_{setup}	Setup time		5	50	25		ns
			10	30	15		
			15	20	10		
t_H	Hold time		5	0	0		ns
			10	0	0		
			15	0	0		
t_{PHL}, t_{PLH}	Propagation delay times:	Strobe to data out	5		130	260	ns
			10		70	140	
			15		50	100	
		Data in to data out	5		105	210	ns
			10		60	120	
			15		45	90	
		Reset to data out	5		90	180	ns
			10		50	100	
			15		40	80	
t_{PHZ}	3-state propagation delay times: output high to high impedance		5		110	220	ns
			10		60	120	
			15		40	80	
t_{PZH}	High impedance to output high		5		90	180	ns
			10		50	100	
			15		35	70	
t_{PLZ}	Output low to high impedance		5		90	180	ns
			10		50	100	
			15		35	70	
t_{PZL}	High impedance to output low		5		90	180	ns
			10		50	100	
			15		35	70	

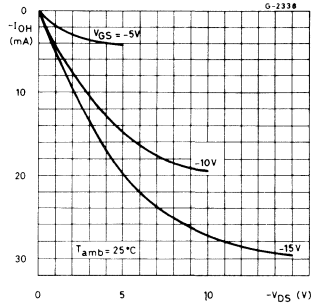
Typical output low (sink) current characteristics



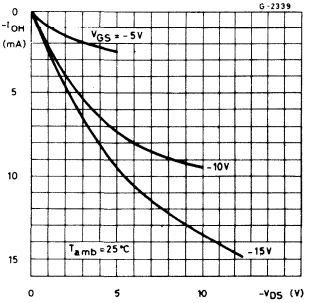
Minimum output low (sink) current characteristics



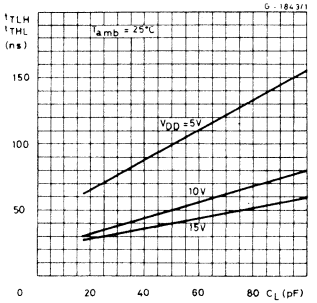
Typical output high (source) current characteristics



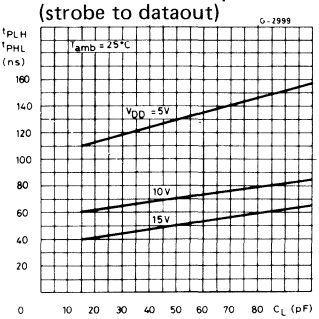
Minimum output high(source) current characteristics



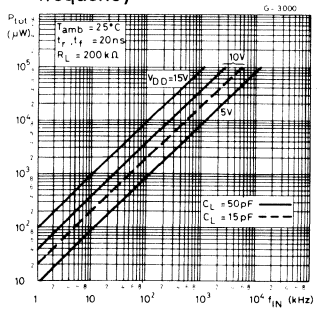
Typical transition time vs. load capacitance



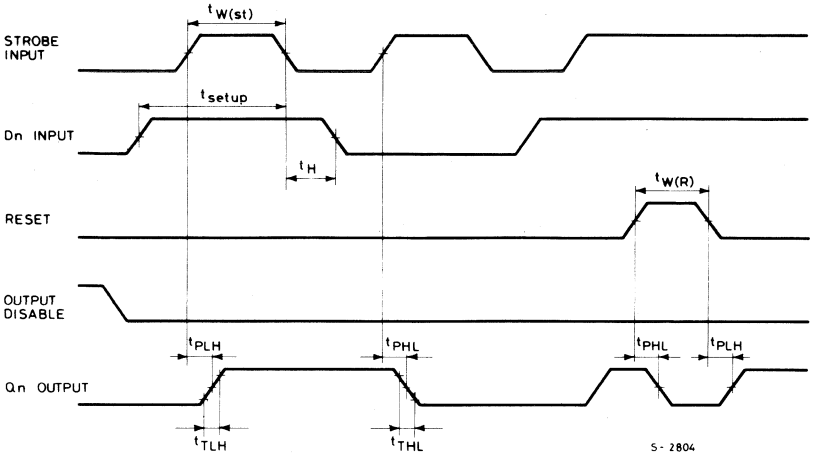
Typical propagation delay time vs. load capacitance (strobe to dataout)



Typical power dissipation vs. frequency

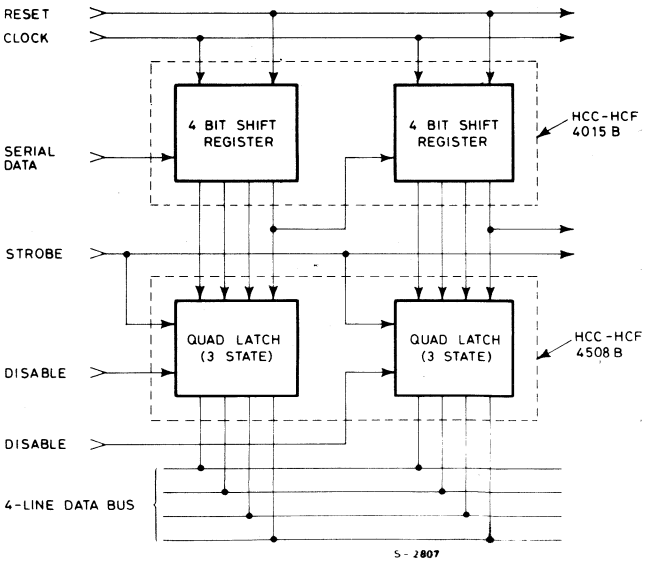


TEST WAVEFORM



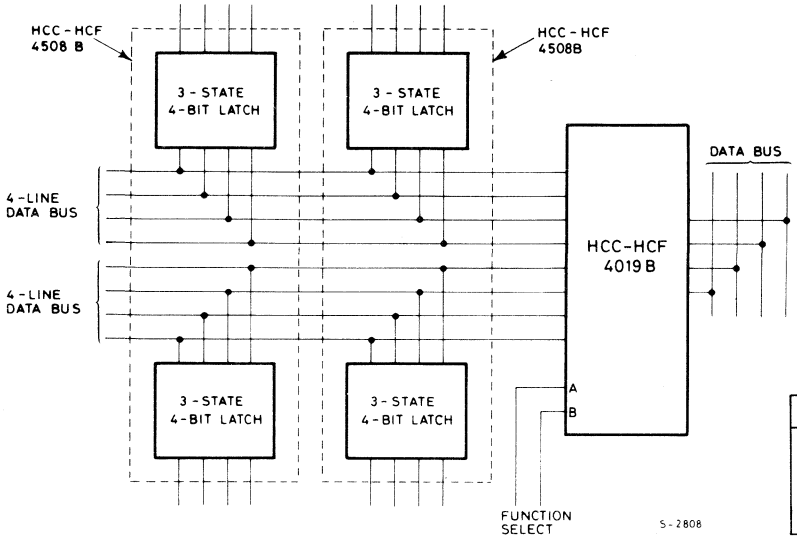
TYPICAL APPLICATIONS

A) Fig. 15 - Bus register



TYPICAL APPLICATIONS (continued)

B) Fig. 16 - Dual multiplexed bus register with function select



A	B	FUNCTION
0	0	Inhibit (all 0)
1	0	Select A Bus
0	1	Select B Bus
1	1	$A_1 + B_1$

COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

PRESETTABLE UP/DOWN COUNTERS

- MEDIUM SPEED OPERATION f_{CL} = 8 MHz TYP. AT 10V
- SYNCHRONOUS INTERNAL CARRY PROPAGATION
- RESET AND PRESET CAPABILITY
- QUIESCENT CURRENT SPECIFIED TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4510B, HCC 4516B** (extended temperature range) and the **HCF 4510B, HCF 4516B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4510B** Presettable BCD Up/Down Counter and the **HCC/HCF 4516B** Presettable Binary Up/Down Counter consist of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as counters. These counters can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. The **HCC/HCF 4510B** will count out of non-BCD counter states in a maximum of two clock pulses in the up mode, and a maximum of four clock pulses in the down mode. If the CARRY-IN input is held low, the counter advances up or down on each positive-going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY-OUT of a less significant stage to the CARRY-IN of a more significant stage. The **HCC/HCF 4510B** and **HCC/HCF 4516B** can be cascaded in the ripple mode by connecting the CARRY-OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY-OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

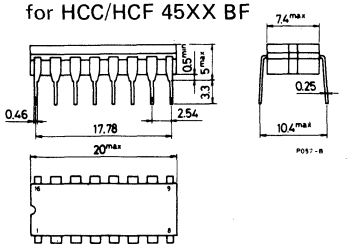
ORDERING NUMBERS:

HCC 45XX BD for dual in-line ceramic package
HCC 45XX BF for dual in-line ceramic package, frit seal
HCC 45XX BK for ceramic flat package
HCF 45XX BE for dual in-line plastic package
HCF 45XX BF for dual in-line ceramic package, frit seal

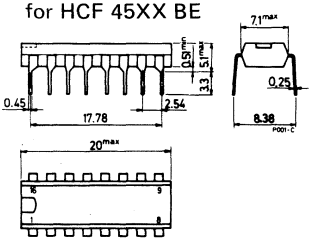
HCC/HCF 4510 B
HCC/HCF 4516 B

MECHANICAL DATA (dimensions in mm)

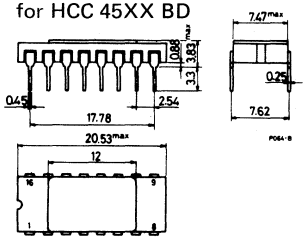
Dual in-line ceramic package
for HCC/HCF 45XX BF



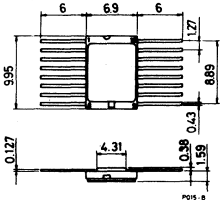
Dual in-line plastic package
for HCF 45XX BE



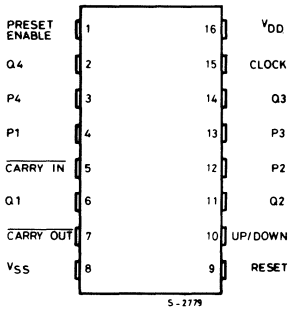
Dual in-line ceramic package
for HCC 45XX BD



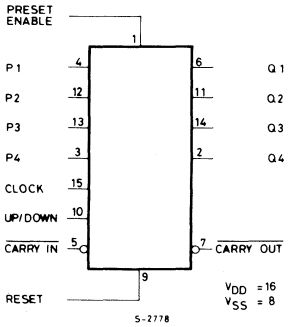
Ceramic flat package
for HCC 45XX BK



CONNECTION DIAGRAMS



FUNCTIONAL DIAGRAM

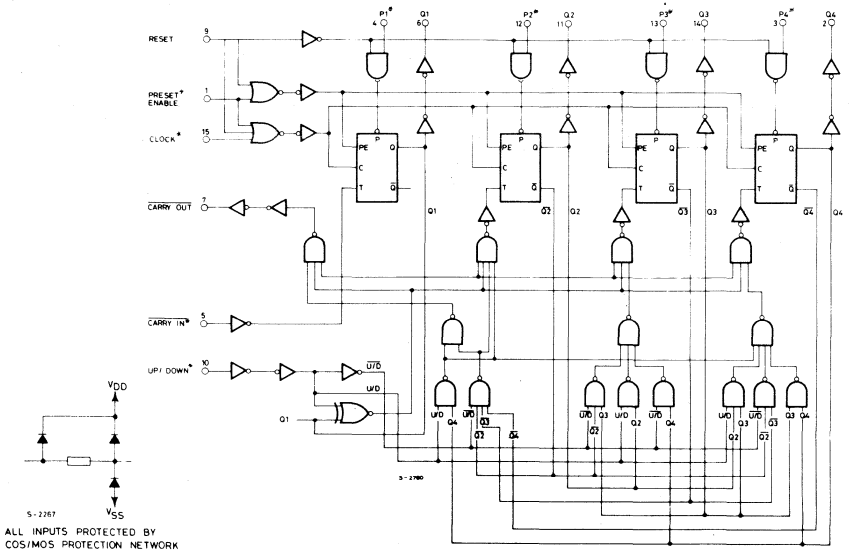


RECOMMENDED OPERATING CONDITIONS

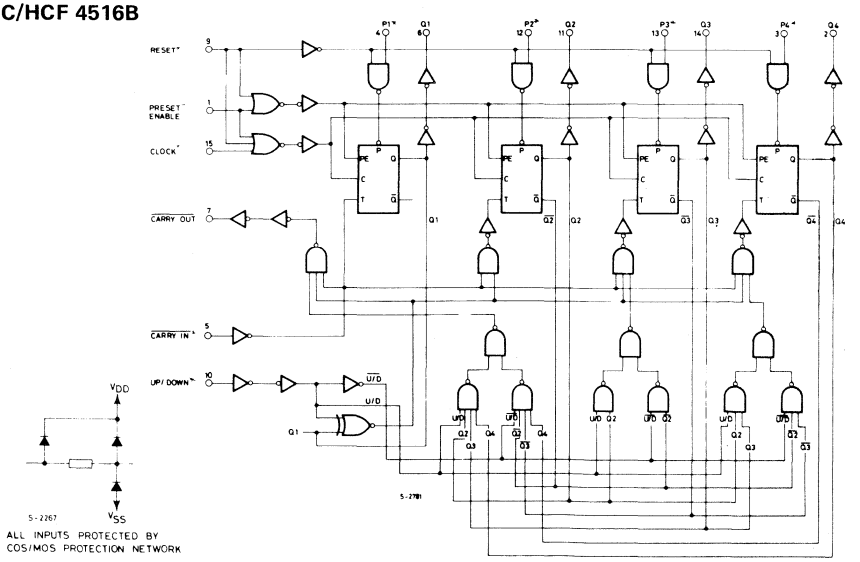
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAMS

for HCC/HCF 4510B

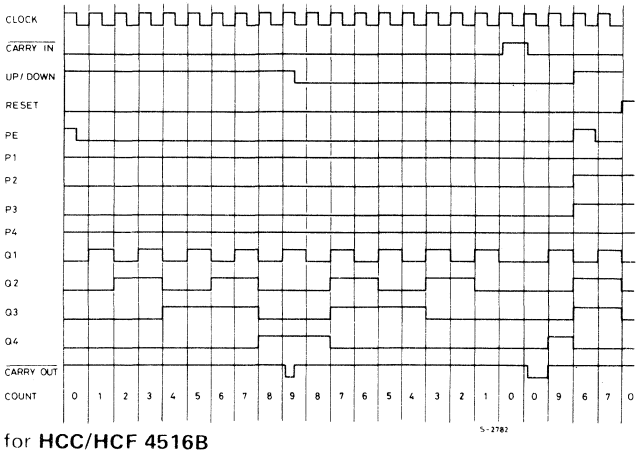


for HCC/HCF 4516B



TIMING DIAGRAMS AND TRUTH TABLE

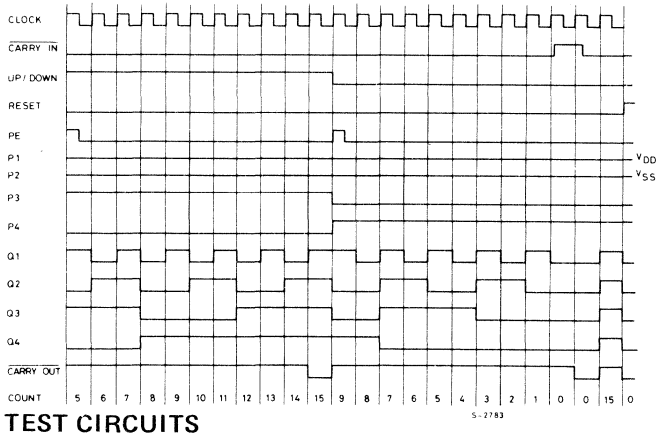
for **HCC/HCF 4510B**



CL	$\overline{CT}$	U/D	PE	R	ACTION
X	1	X	0	0	NO COUNT
⌐	0	1	0	0	COUNT UP
⌐	0	0	0	0	COUNT DOWN
X	X	X	1	0	PRESET
X	X	X	X	1	RESET

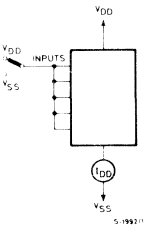
X = Don't care

for **HCC/HCF 4516B**

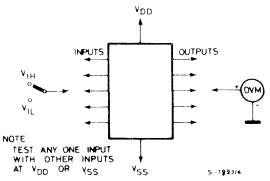


TEST CIRCUITS

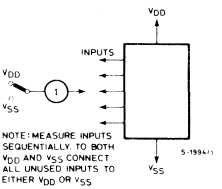
Quiescent device current



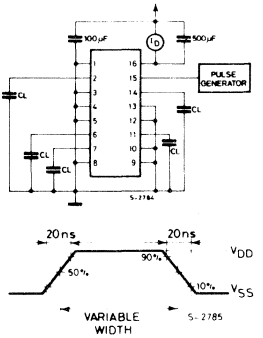
Noise immunity



Input leakage current



Power dissipation and input waveform



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

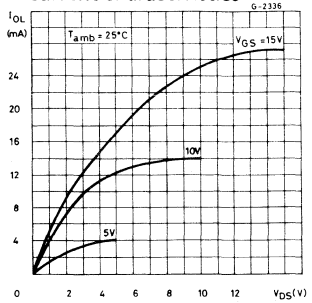
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation delay time clock to Q output		5		200	400	ns
			10		100	200	
			15		75	150	
t_{PHL}, t_{PLH}	Propagation delay time preset or reset to Q output		5		210	420	ns
			10		105	210	
			15		80	160	
t_{PHL}, t_{PLH}	Propagation delay time clock to carry out		5		240	480	ns
			10		120	240	
			15		90	180	
t_{PHL}, t_{PLH}	Propagation delay time carry in to carry out		5		125	250	ns
			10		60	120	
			15		50	100	
t_{PHL}, t_{PLH}	Propagation delay time preset or reset to carry out		5		320	640	ns
			10		160	320	
			15		125	250	
t_{THL}, t_{TLH}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
f_{max}	Max. clock frequency		5	2	4		MHz
			10	4	8		
			15	5.5	11		
t_W	Clock pulse width		5	150			ns
			10	75			
			15	60			
	• Preset enable or reset removal time		5	150			ns
			10	80			
			15	60			
t_r t_f	* Clock rise and fall time		5			15	μs
			10			5	
			15			5	
t_{setup}	Carry in setup time		5	130			ns
			10	60			
			15	45			
t_{setup}	Up-down setup time		5	360			ns
			10	160			
			15	110			
t_W	Preset enable or reset pulse width		5	220			ns
			10	100			
			15	75			

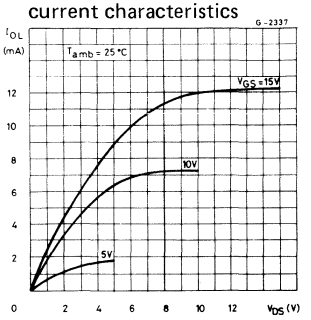
• Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time).

* If more than unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 15 pF and the transition time of the carry output driving stage for the estimated capacitive load.

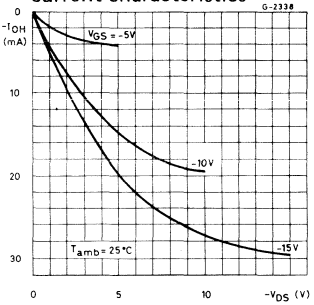
Typical output low (sink) current characteristics



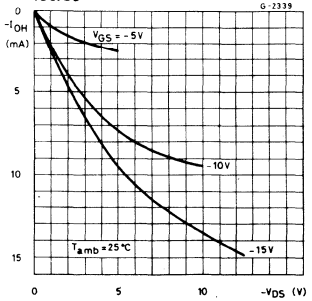
Minimum output low (sink) current characteristics



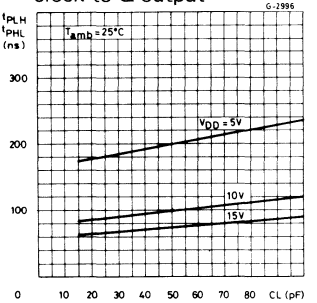
Typical output high (source) current characteristics



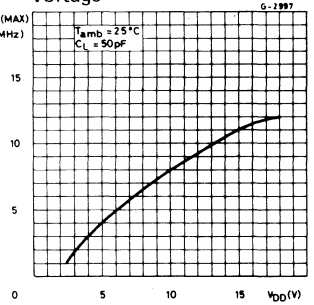
Minimum output high (source) current characteristics



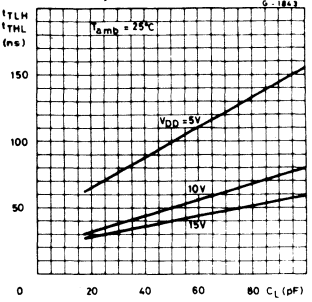
Typical propagation delay time vs. load capacitance for clock to Q output



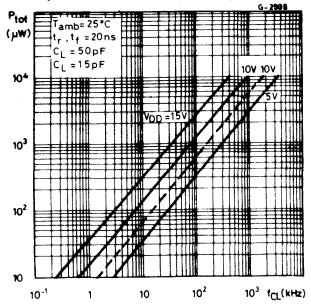
Typical maximum clock input frequency vs. supply voltage



Typical transition time vs. load capacitance

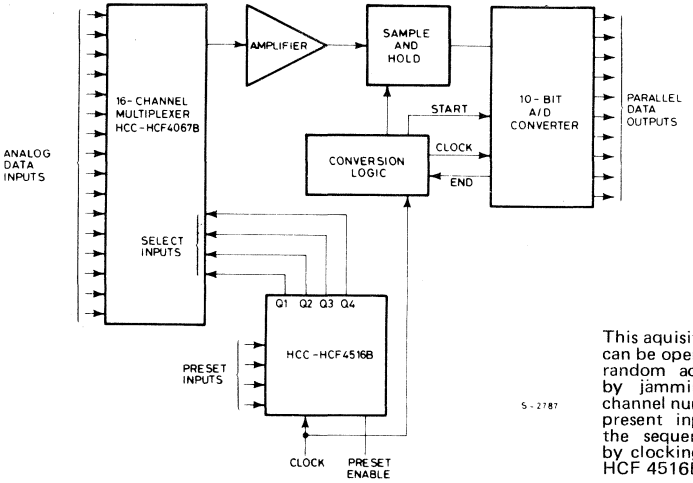


Typical dynamic power dissipation vs. frequency



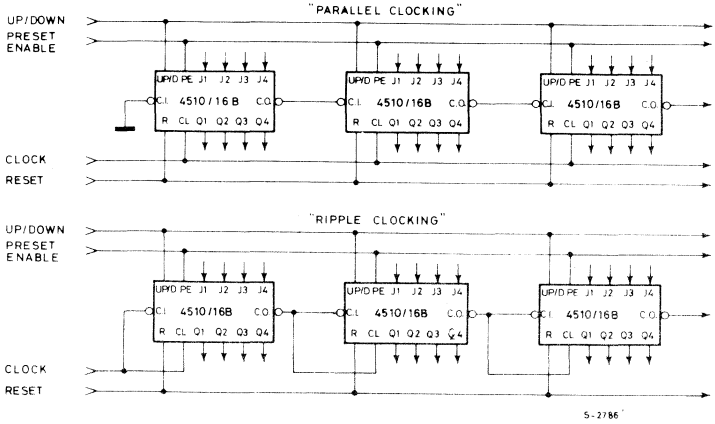
TYPICAL APPLICATIONS

Typical 16-channel, 10 bit data aquisition system



This aquisition system can be operated in the random access mode by jamming in the channel number at the present inputs, or in the sequential mode by clocking the HCC/HCF 4516B.

Cascading counter packages



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

- HIGH-OUTPUT-SOURCING CAPABILITY (up to 25 mA)
- INPUT LATCHES FOR BCD CODE STORAGE
- LAMP TEST AND BLANKING CAPABILITY
- 7-SEGMENT OUTPUTS BLANKED FOR BCD INPUT CODES > 1001
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT LEAKAGE OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4511B** (extended temperature range) and the **HCF 4511B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4511B** types are BCD-to-7-segment latch decoder drivers constructed with COS/MOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of COS/MOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the **HCC/HCF 4511B** types to drive LED's and other displays directly.
Lamp Test ($\overline{LT}$), Blanking ($\overline{BL}$), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signal may be multiplexed and displayed when external multiplexing circuitry is used.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

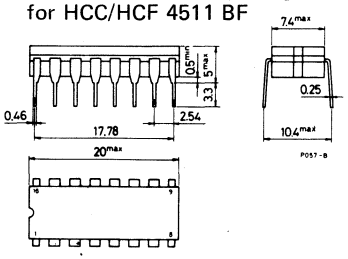
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

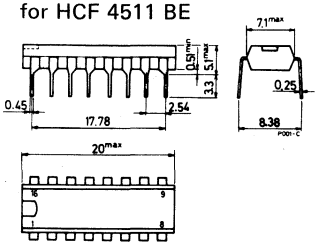
HCC 4511 BD for dual in-line ceramic package
HCC 4511 BF for dual in-line ceramic package, frit seal
HCC 4511 BK for ceramic flat package
HCF 4511 BE for dual in-line plastic package
HCF 4511 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

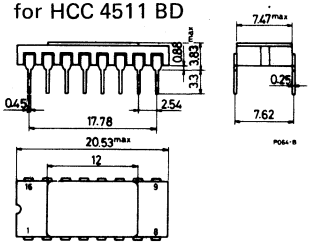
Dual in-line ceramic package for HCC/HCF 4511 BF



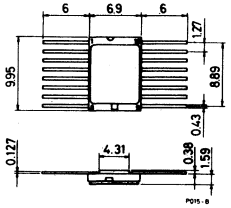
Dual in-line plastic package for HCF 4511 BE



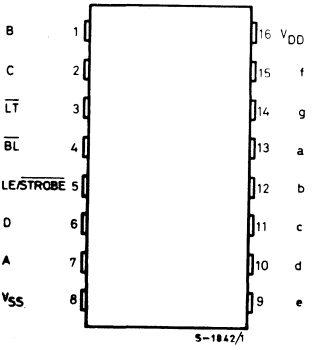
Dual in-line ceramic package for HCC 4511 BD



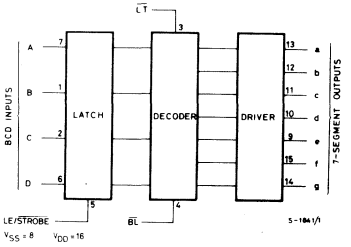
Ceramic flat package for HCC 4511 BK



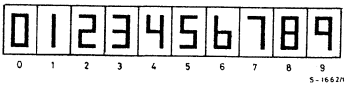
CONNECTION DIAGRAM

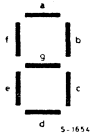


FUNCTIONAL DIAGRAM



DISPLAY

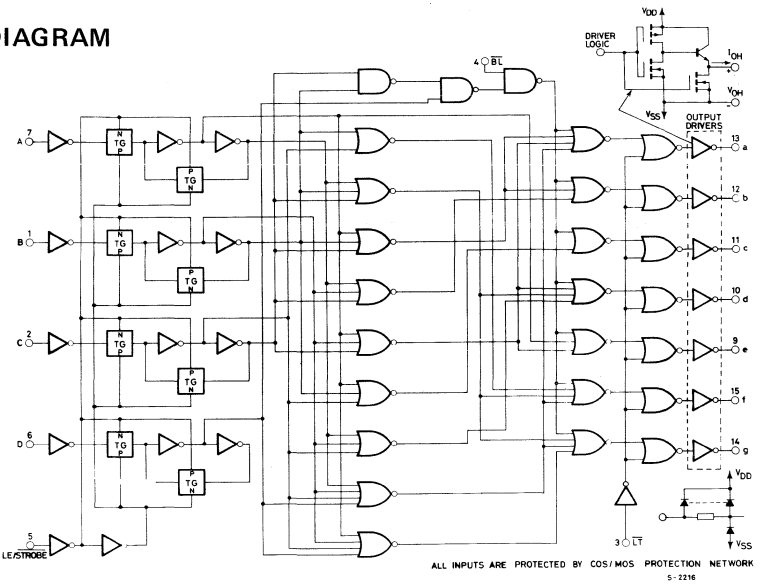




RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18 V
V_I	Input voltage	0 to V_{DD} V
T_{op}	Operating temperature: for **HCC** types	-55 to 125 °C
	for **HCF** types	-40 to 85 °C

LOGIC DIAGRAM

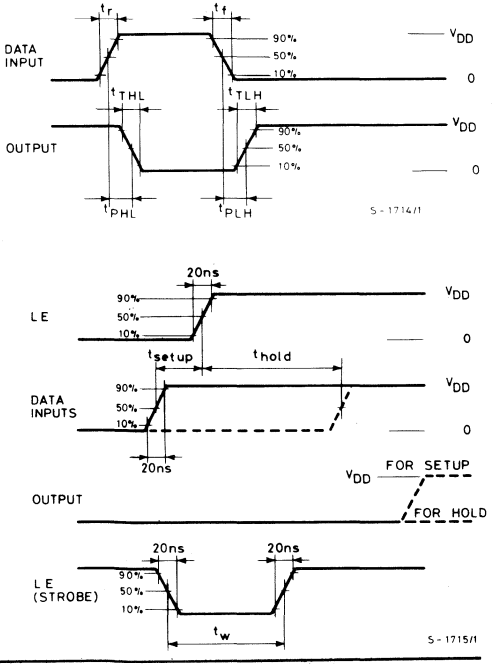


TRUTH TABLE

LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X = Don't care
* = Depends on BCD code previously applied when LE= 0
Note: Display is blank for all illegal input codes (BCD > 1001)

WAVEFORMS



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

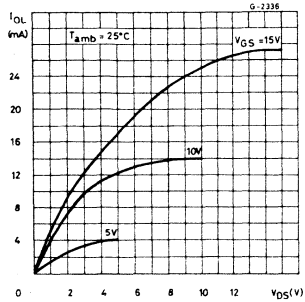
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_{OH}\|$ (mA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current					5		5		0.04	5		150	μA
						10		10		0.04	10		300	
						15		20		0.04	20		600	
						20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5			5	4		4.1	4.55		4.2		V
			0/10			10	9		9.1	9.55		9.2		
			0/15			15	14		14.1	14.55		14.2		
V_{OL}	Output low voltage		5/0			5		0.05			0.05		0.05	V
			10/0			10		0.05			0.05		0.05	
			15/0			15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/3.8		5	3.5		3.5			3.5		V
				1/8.8		10	7		7			7		
				1.5/13.8		15	11		11			11		
V_{IL}	Input low voltage			3.8/0.5		5		1.5			1.5		1.5	V
				8.8/1		10		3			3		3	
				13.8/1.5		15		4			4		4	
V_{OH}	Output drive voltage				0	5	4		4.10	4.55		4.20		V
					5					4.25				
					10		3.80		3.90	4.10		3.90		
					15					3.95		3.50		
					20		3.55		3.40	3.75				
					25		3.40		3.10	3.55				
					0	10	9		9.10	9.55		9.20		
					5					9.25				
					10		8.85		9	9.15				
					15					9.05				
					20		8.70		8.60	8.90		8.40		
					25		8.60		8.30	8.75				
					0	15	14		14.10	14.55		14.20		V
					5					14.30				
					10		13.90		14	14.20		14		
					15					14.10				
					20		13.75		13.70	13.95		13.50		
					25		13.65		13.50	13.80		13.10		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18	0/18		18		± 0.1		± 10^{-5}	± 0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = − 55°C for **HCC** device; −40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

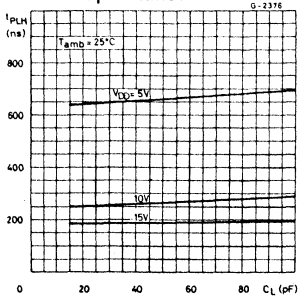
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}	Propagation delay time (Data)	5		520	1040	ns
		10		210	420	
		15		150	300	
t_{PLH}	Propagation delay time (Data)	5		660	1320	ns
		10		260	520	
		15		180	360	
t_{PHL}	Propagation delay time ($\overline{BL}$)	5		350	700	ns
		10		175	350	
		15		125	250	
t_{PLH}	Propagation delay time ($\overline{BL}$)	5		400	800	ns
		10		175	350	
		15		150	300	
t_{PHL}	Propagation delay time ($\overline{LT}$)	5		250	500	ns
		10		125	250	
		15		85	170	
t_{PLH}	Propagation delay time ($\overline{LT}$)	5		150	300	ns
		10		75	150	
		15		50	100	
t_{TLH}	Transition time	5		40	100	ns
		10		30	75	
		15		20	65	
t_{THL}	Transition time	5		125	310	ns
		10		75	185	
		15		65	160	
t_{setup}	Setup time	5	150	75		ns
		10	70	35		
		15	40	20		
t_{hold}	Hold time	5	0	-75		ns
		10	0	-35		
		15	0	-20		
t_W	Strobe pulse width	5	400	200		ns
		10	160	80		
		15	100	50		

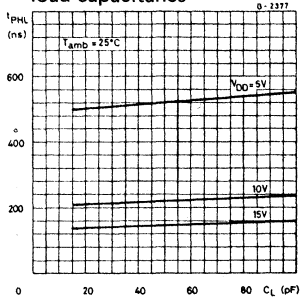
Typical output low (sink) current characteristics



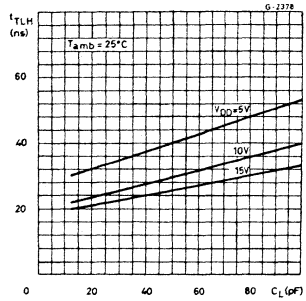
Typical data-to-output,low-to-high-level propagation delay time as a function of load capacitance



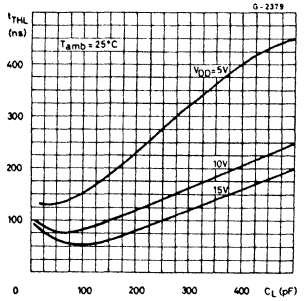
Typical data-to-output,high-to-low-level propagation delay time as a function of load capacitance



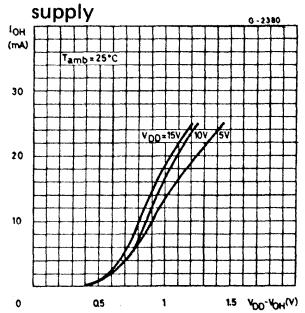
Typical low-to-high level transition time as a function of load capacitance



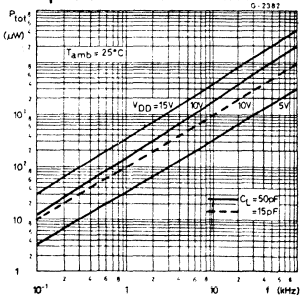
Typical high-to-low transition time as a function of load capacitance



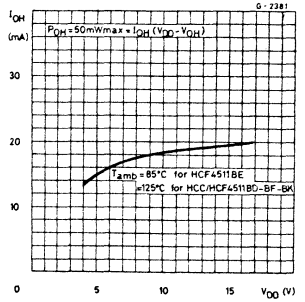
Typical voltage drop (V_{DD} to output) vs. output source current as a function of supply



Typical dynamic power dissipation characteristics



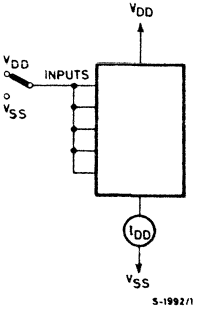
Derated static output current per output



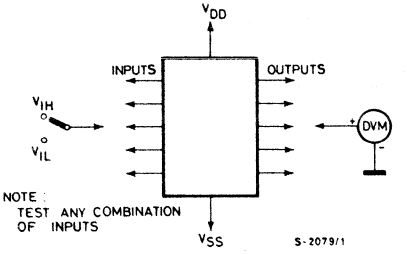
Maximum continuous derated output current I_{OH} applies to a single output with all other outputs sourcing an equal amount of current at the supply voltages shown. Operation above the derating curve is not recommended.

TEST CIRCUITS

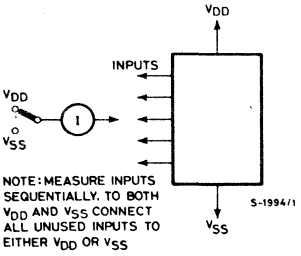
Quiescent device current



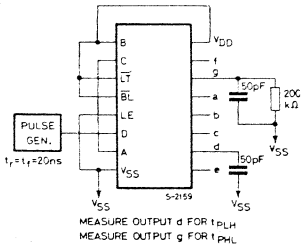
Noise immunity



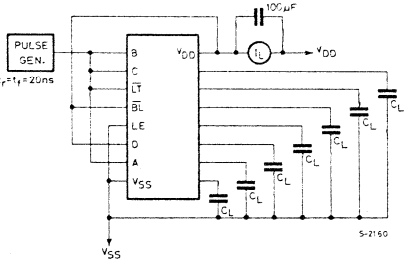
Input leakage current



Data propagation delay

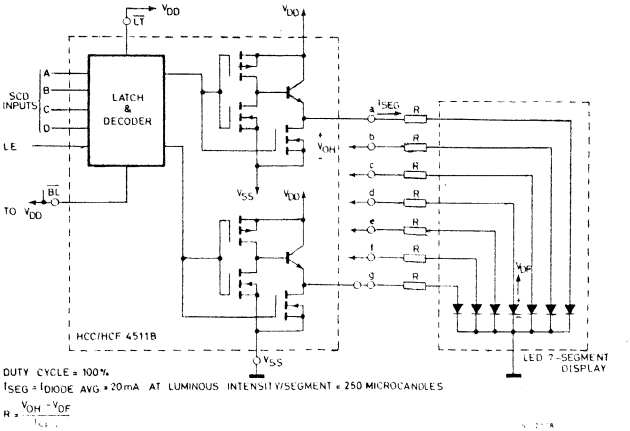


Dynamic power dissipation



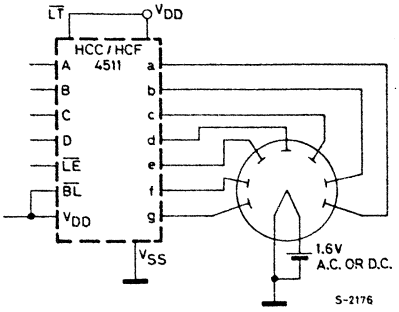
APPLICATIONS (Interfacing with various displays)

Driving common-cathode 7-segment LED displays



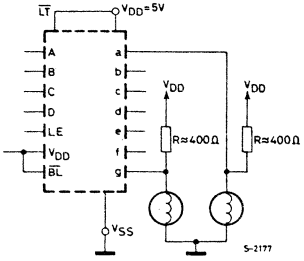
APPLICATIONS (continued)

Driving low-voltage fluorescent displays



A medium-brightness intensity display can be obtained with low-voltage fluorescent displays such as the Tung-Sot Digivac S/G Series.

Driving incandescent displays



2 of 7 Segments Shown Connected

Resistors R from V_{DD} to each 7-segment driver output are chosen to keep all Numitron segments slightly on and warm.

COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

8-CHANNEL DATA SELECTOR

- 3-STATE OUTPUT
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4512B** (extended temperature range) and **HCF 4512B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package.
The **HCC/HCF 4512B** is an 8-channel data selector featuring a three-state output that can interface directly with, and drive, data lines of bus-oriented systems.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

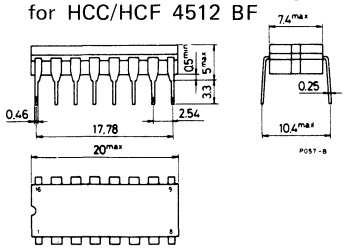
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS;

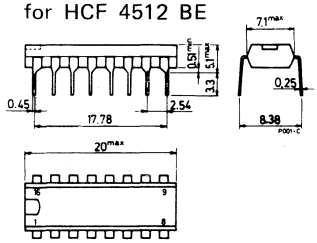
HCC 4512 BD for dual in-line ceramic package
HCC 4512 BF for dual in-line ceramic package, frit seal
HCC 4512 BK for ceramic flat package
HCF 4512 BE for dual in-line plastic package
HCF 4512 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

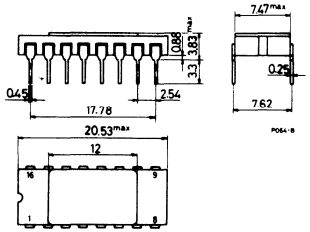
Dual in-line ceramic package for HCC/HCF 4512 BF



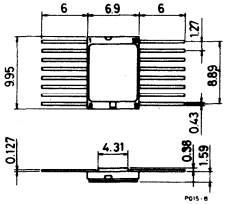
Dual in-line plastic package for HCF 4512 BE



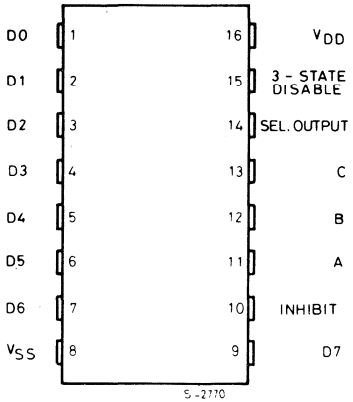
Dual in-line ceramic package for HCC 4512 BD



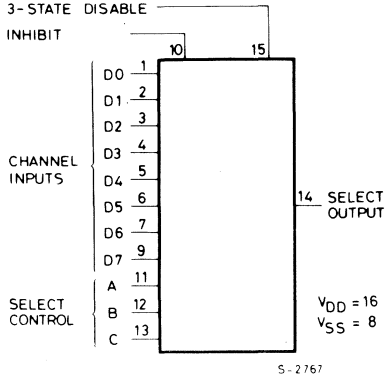
Ceramic flat package for HCC 4512 BK



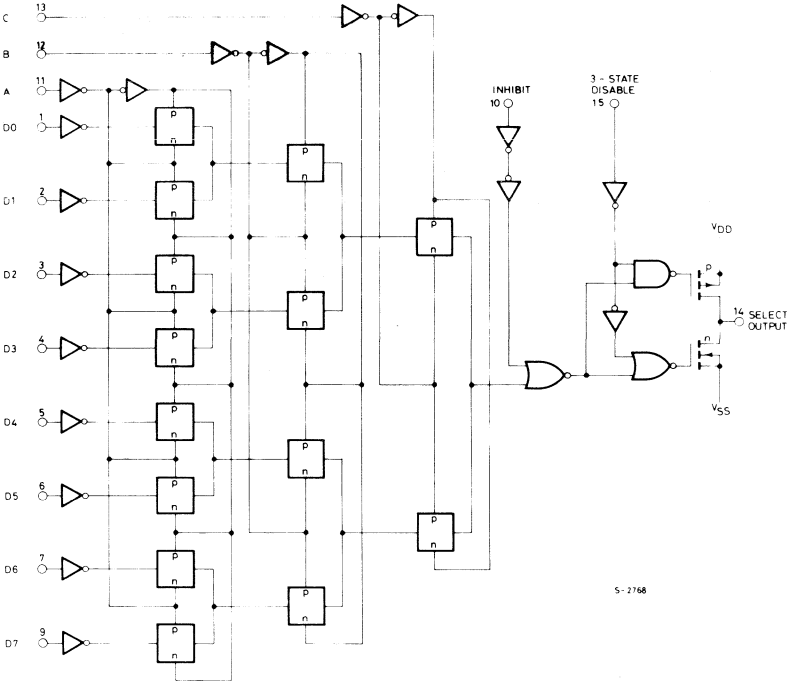
CONNECTION DIAGRAM

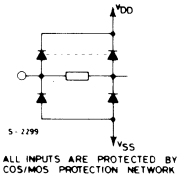


FUNCTIONAL DIAGRAM



LOGIC DIAGRAM





TRUTH TABLE

SEL. CONT.			INH.	3-STATE DISABLE	SEL. OUTPUT
A	B	C			
0	0	0	0	0	D 0
1	0	0	0	0	D 1
0	1	0	0	0	D 2
1	1	0	0	0	D 3
0	0	1	0	0	D 4
1	0	1	0	0	D 5
0	1	1	0	0	D 6
1	1	1	0	0	D 7
X	X	X	1	0	0
X	X	X	X	1	High Z

1 = High Level
0 = Low Level
X = Don't Cave

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

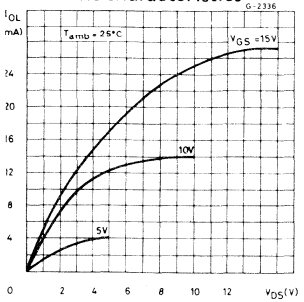
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		± 0.1		$\pm 10^{-5}$	± 0.1		± 1	μA
$I_{O\ max}$	3-state output leakage current		0/18	0/18		18		± 0.4		$\pm 10^{-4}$	± 0.4		± 12	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

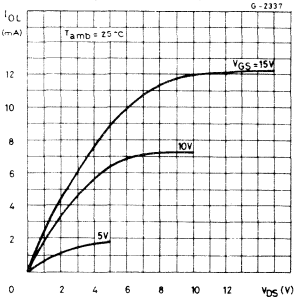
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
	V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH} Propagation delay time inhibit to output	5		140	280	ns
	10		70	140	
	15		50	100	
t_{PHL}, t_{PLH} Propagation delay time "A" select to output	5		200	400	ns
	10		85	170	
	15		60	120	
t_{PHL}, t_{PLH} Propagation delay time data to output	5		180	360	ns
	10		75	150	
	15		55	110	
t_{PZL}, t_{PLZ}, t_{PHZ}, t_{PZH} 3-State disable delay time	5		60	120	ns
	10		30	60	
	15		20	40	
t_{THL}, t_{TLH} Transition time	5		100	200	ns
	10		50	100	
	15		40	80	

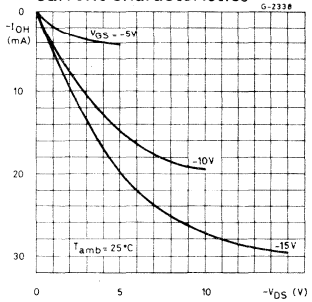
Typical output low (sink) current characteristics



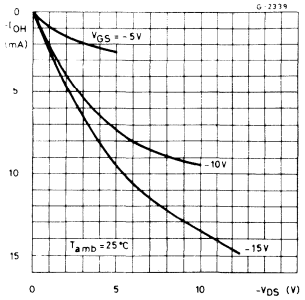
Minimum output low (sink) current characteristics



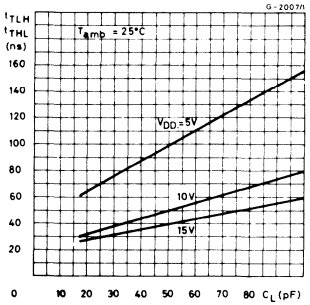
Typical output high (source) current characteristics



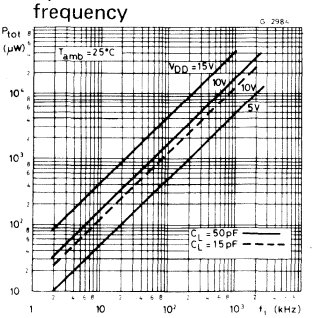
Minimum output high(source) current characteristics



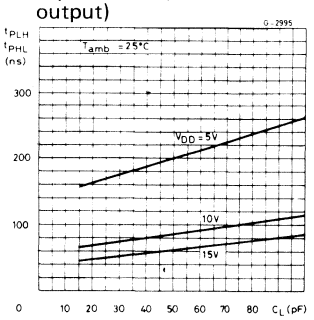
Typical transition time vs. load capacitance



Typical dynamic power dissipation as a function of frequency

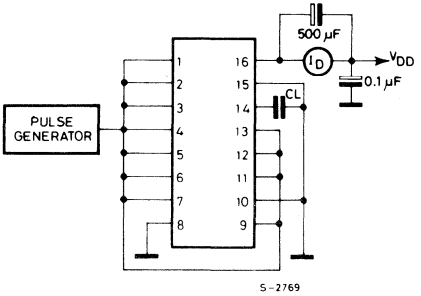


Typical propagation delay time as a function of load capacitance ("A" select to output)

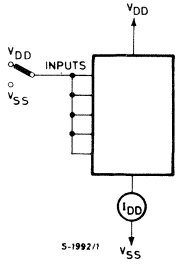


TEST CIRCUITS

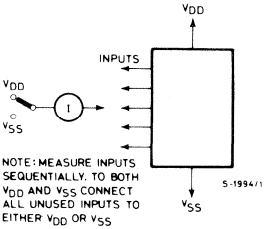
Dynamic power dissipation test circuit



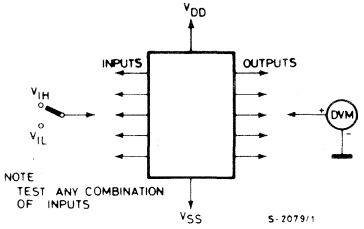
Quiescent device current test circuit



Input current test circuit



Input voltage test circuit



COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

4-BIT LATCH/4-TO-16 LINE DECODER:

HCC/HCF 4514B OUTPUT "HIGH" ON SELECT
HCC/HCF 4515B OUTPUT "LOW" ON SELECT

- QUIESCENT CURRENT SPECIFIED TO 20V
- MAX. INPUT LEAKAGE CURRENT 1 μA @18V (FULL PACKAGE - TEMP. RANGE)
- STROBED INPUT LATCH
- INHIBIT CONTROL

The **HCC 4514B/HCC 4515B** (extended temperature range) and the **HCF 4514B/HCF 4515B** (intermediate temperature range) are monolithic integrated circuits available in 24-lead dual in-line plastic and ceramic slam package. The **HCC/HCF 4514B/4515B** consisting of a 4-bit strobed latch and a 4 to 16 line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0 (**HCC/HCF 4514B**) or 1 (**HCC/HCF 4515B**) regardless of the state of the data or strobe inputs. The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

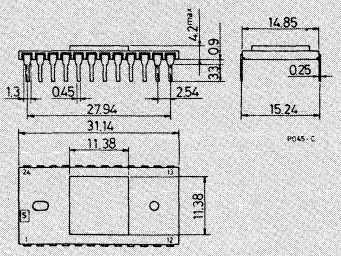
ORDERING NUMBERS:

HCC 45XX BD for dual in-line ceramic slam package
HCF 45XX BD for dual in-line ceramic slam package
HCF 45XX BE for dual in-line plastic package

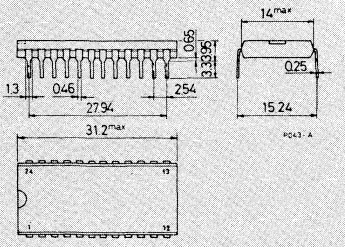
MECHANICAL DATA

dimensions in mm

Dual in-line ceramic slam package
for HCC/HCF 45XX BD

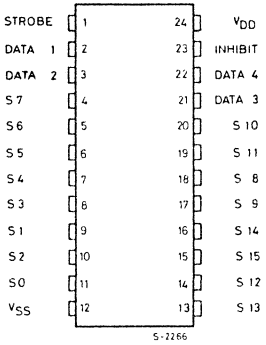


Dual in-line plastic package
for HCF 45XX BE

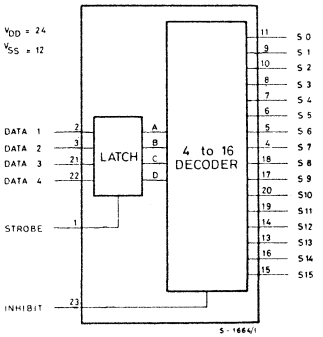


HCC/HCF 4514 B
HCC/HCF 4515 B

CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM



DECODER TRUTH TABLE*

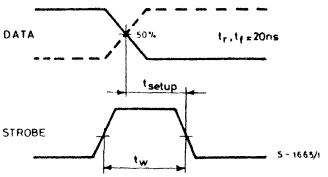
INHIBIT	DATA INPUTS				SELECTED OUTPUT HCC/HCF 4514B= Logic 1 (High) HCC/HCF 4515B= Logic 0 (Low)
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs= 0, HCC/HCF 4514B All Outputs= 1; HCC/HCF 4515B

X = Don't Care
1 = high
0 = low

*Strobe = 1

WAVEFORMS

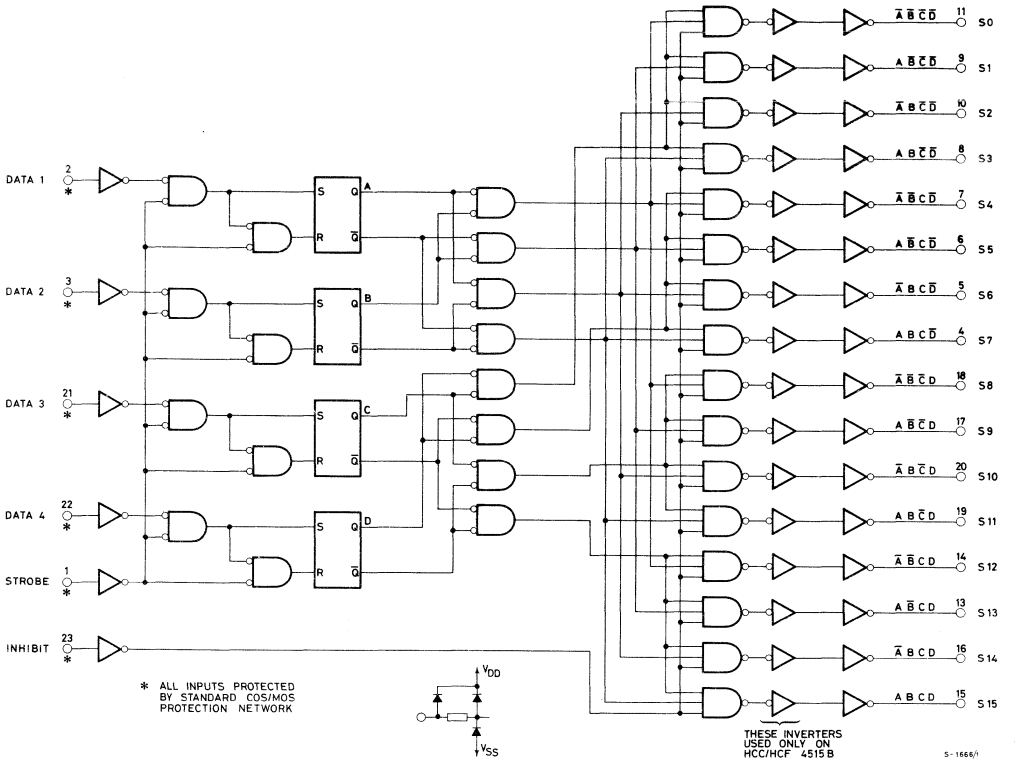
Setup time and strobe pulse width



RECOMMENDED OPERATING CONDITIONS

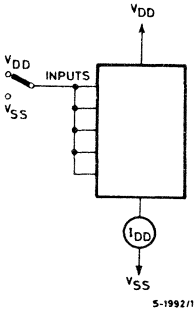
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM

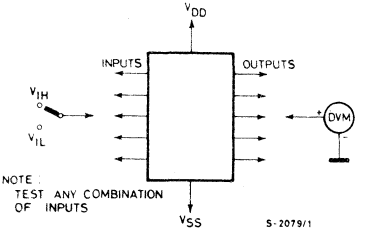


TEST CIRCUITS

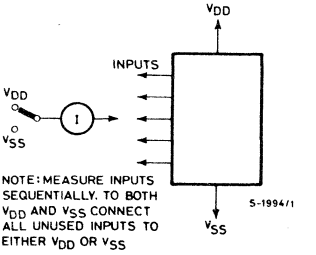
Quiescent device current



Noise immunity



Input leakage current



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

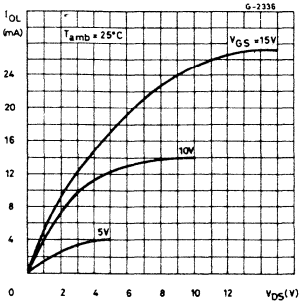
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		1		0.02	5		150	μA
			0/10			10		2		0.02	10		300	
			0/15			15		4		0.02	20		600	
			0/20			20		20		0.04	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

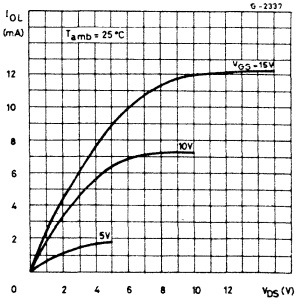
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions		Values			Unit
			V_{DD} V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation delay time	Strobe or data	5		485	970	ns
			10		185	370	
			15		135	270	
		Inhibit	5		250	500	
			10		110	220	
			15		85	170	
t_{THL}, t_{THL}	Transition time		5		100	200	ns
			10		50	100	
			15		40	80	
t_w	Strobe pulse width		5	250	125		ns
			10	100	50		
			15	75	40		
t_{setup}	Setup time		5	150	75		ns
			10	70	35		
			15	40	20		

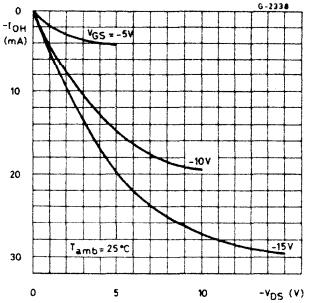
Typical output low (sink) current characteristics



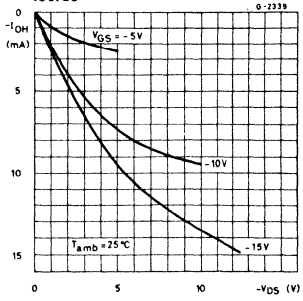
Minimum output low (sink) current characteristics



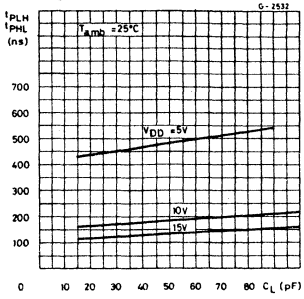
Typical output high (source) current characteristics



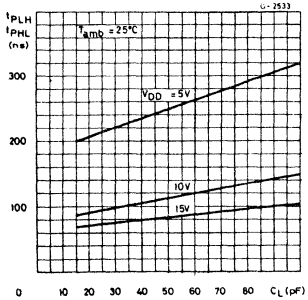
Minimum output high (source) current characteristics



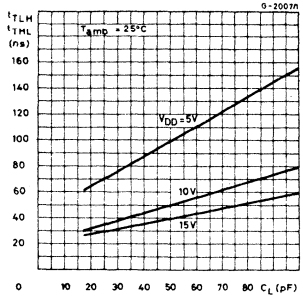
Typical strobe or data propagation delay time vs. load capacitance



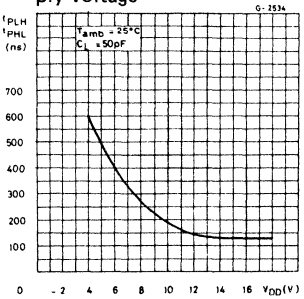
Typical inhibit propagation delay time vs. load capacitance



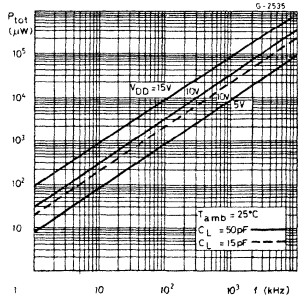
Typical transition time vs. load capacitance



Typical strobe or data propagation delay time vs. supply voltage



Typical power dissipation vs. frequency



COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

DUAL UP-COUNTERS: HCC/HCF 4518B DUAL BCD UP-COUNTER
HCC/HCF 4520B DUAL BINARY UP-COUNTER

- MEDIUM-SPEED OPERATION - 6 MHz TYP. CLOCK FREQUENCY AT 10V
- POSITIVE - OR NEGATIVE - EDGE TRIGGERING
- SYNCHRONOUS INTERNAL CARRY PROPAGATION
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4518B/4520B** (extended temperature range) and **HCF 4518B/4520B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4518B** Dual BCD Up Counter and **HCC/HCF 4520B** Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the Enable input is maintained "high" and the counter advances on each positive-going transition of the Clock. The counters are cleared by high levels on their Reset lines. The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the clock input of the latter is held low.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

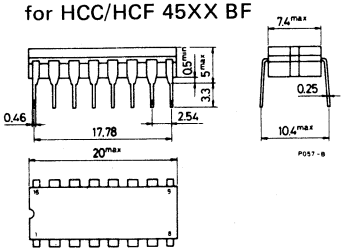
ORDERING NUMBERS:

HCC 45XX BD for dual in-line ceramic package
HCC 45XX BF for dual in-line ceramic package, frit seal
HCC 45XX BK for ceramic flat package
HCF 45XX BE for dual in-line plastic package
HCF 45XX BF for dual in-line ceramic package, frit seal

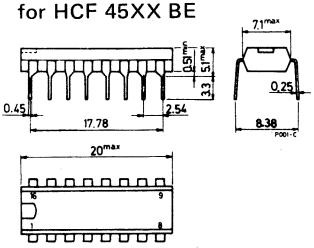
HCC/HCF 4518 B
HCC/HCF 4520 B

MECHANICAL DATA (dimensions in mm)

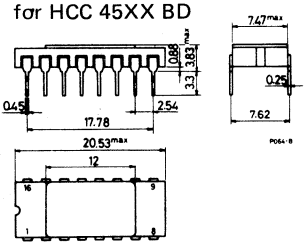
Dual in-line ceramic package
for HCC/HCF 45XX BF



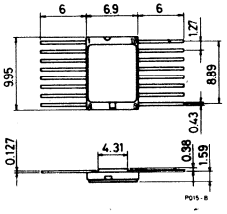
Dual in-line plastic package
for HCF 45XX BE



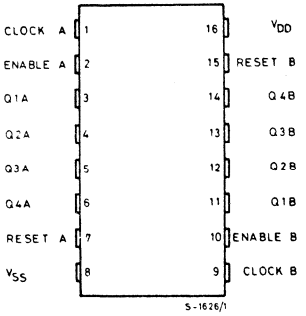
Dual in-line ceramic package
for HCC 45XX BD



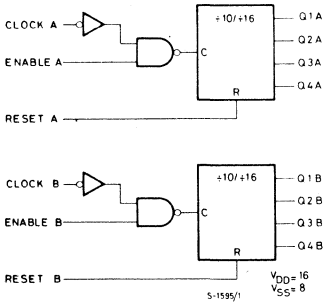
Ceramic flat package
for HCC 45XX BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

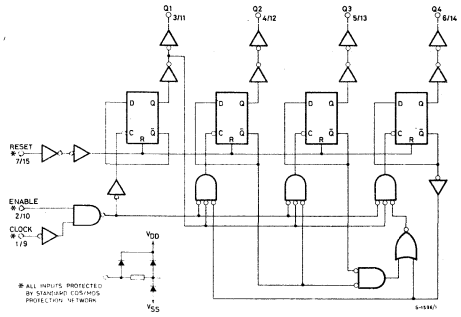


RECOMMENDED OPERATING CONDITIONS

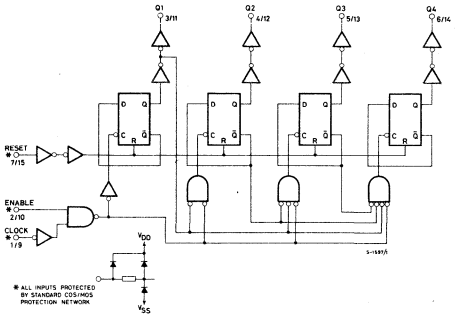
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAMS (for one of two identical counter)

Decade counter for 4518B



Binary counter for 4520B

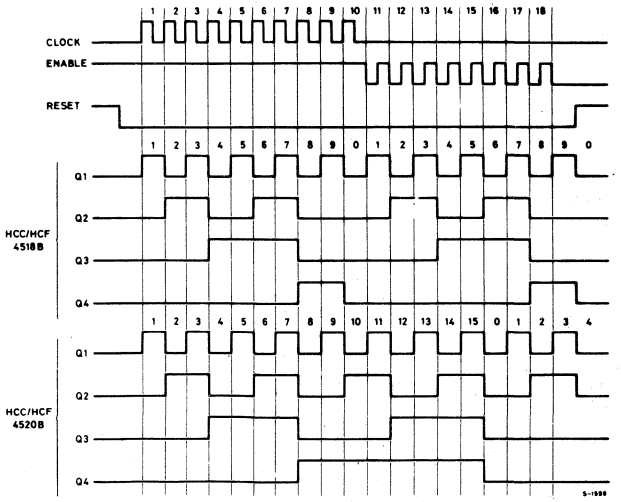


TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⟋	1	0	Increment Counter
0	⟍	0	Increment Counter
⟍	X	0	No Change
X	⟋	0	No Change
⟋	0	0	No Change
1	⟍	0	No Change
X	X	1	Q1 thru Q4 = 0

X= Don't Care 1= High State 0= Low State

TIMING DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

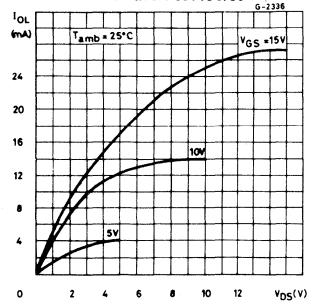
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

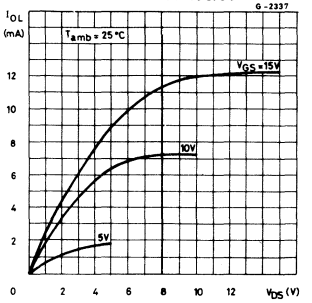
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time (Clock or Enable to output)	5		280	560	ns
		10		115	230	
		15		80	160	
t_{PLH}, t_{PHL}	Propagation delay time (Reset to output)	5		330	650	ns
		10		130	225	
		15		90	170	
t_{TLH}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_W	Clock pulse width	5	200	100		ns
		10	100	50		
		15	70	35		
t_W	Reset pulse width	5	250	125		ns
		10	110	55		
		15	80	40		
t_W	Enable pulse width	5	400	200		ns
		10	200	100		
		15	140	70		
t_r, t_f	Clock or enable rise and fall time	5			15	μs
		10			15	
		15			5	
f_{max}	Maximum clock frequency	5	1,5	3		MHz
		10	3	6		
		15	4	8		

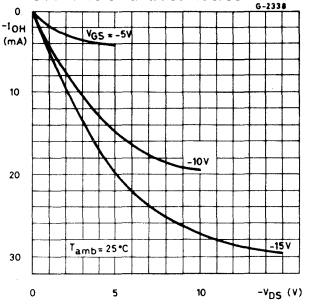
Typical output low (sink) current characteristics



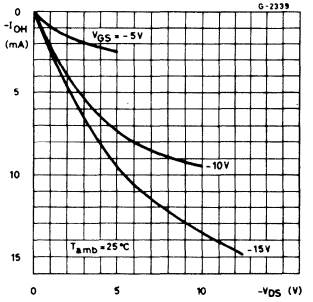
Minimum output low (sink) current characteristics



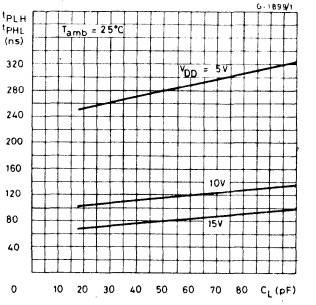
Typical output high (source) current characteristics



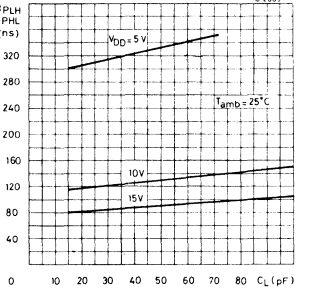
Minimum output high (source) current characteristics



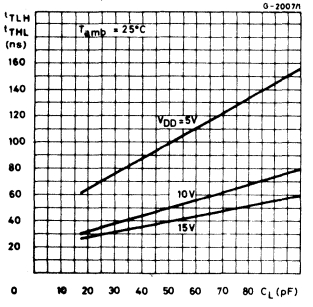
Typical propagation delay vs. load capacitance, reset to output



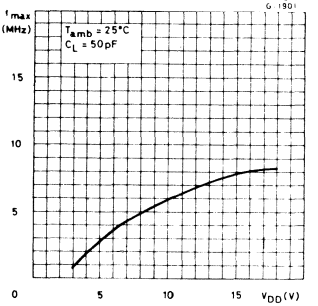
Typical propagation delay time vs. load capacitance, clock or enable to output



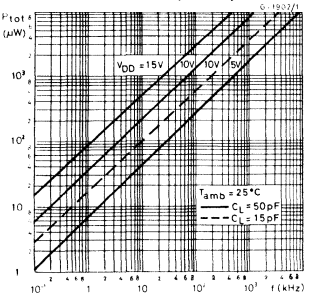
Typical transition time vs. load capacitance



Typical maximum-clock frequency vs, supply voltage

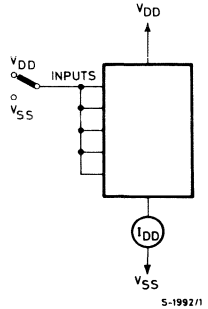


Typical power dissipation/ counter vs. frequency

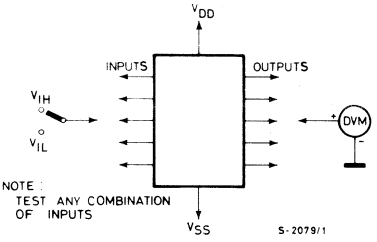


TEST CIRCUITS

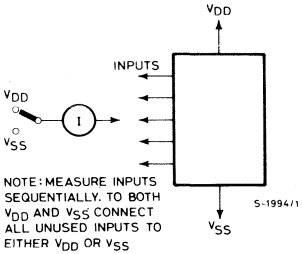
Quiescent device current



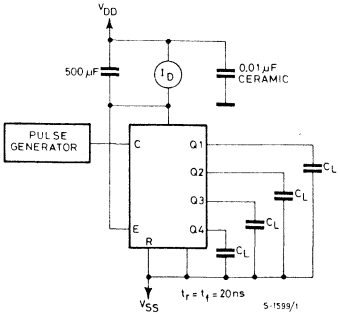
Noise immunity



Input leakage current

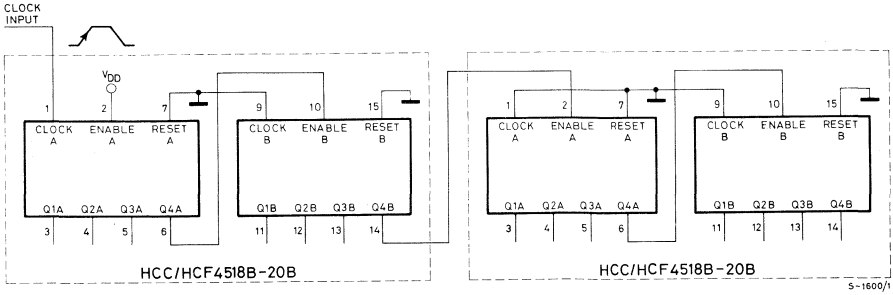


Dynamic power dissipation



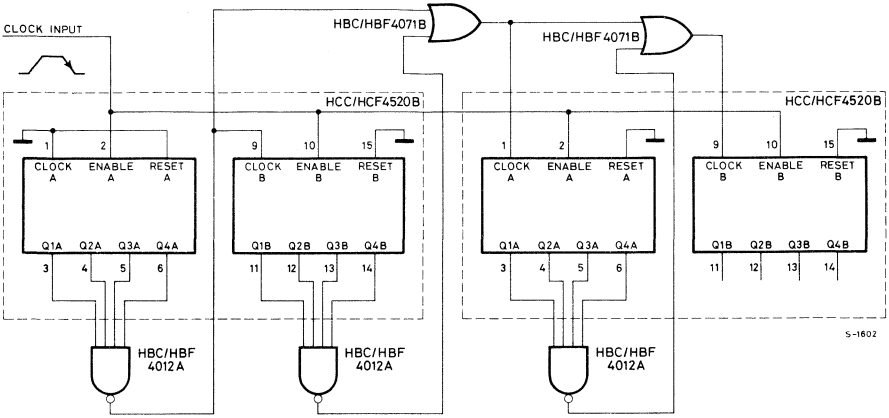
TYPICAL APPLICATIONS

Ripple cascading of four counters with positive-edge triggering



TYPICAL APPLICATIONS (continued)

Synchronous cascading of four binary counters with negative-edge triggering



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

BCD RATE MULTIPLIER

- CASCADABLE IN MULTIPLES OF 4-BITS
- SET TO 9 INPUT AND 9 DETECT OUTPUT
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4527B** (extended temperature range) and **HCF 4527B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package, and ceramic flat package.
The **HCC/HCF 4527** is a low-power 4-bit digital rate multiplier that provides an output-pulse rate which is the clock-input-pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses foe every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

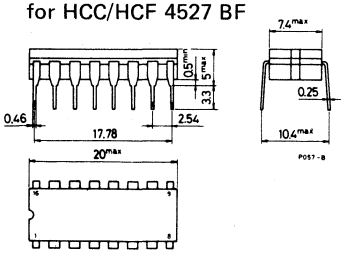
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

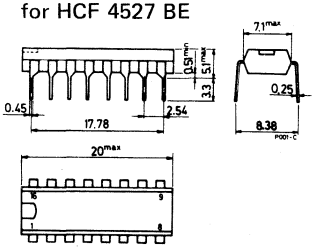
HCC 4527 BD for dual in-line ceramic package
HCC 4527 BF for dual in-line ceramic package, frit seal
HCC 4527 BK for ceramic flat package
HCF 4527 BE for dual in-line plastic package
HCF 4527 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA(dimensions in mm)

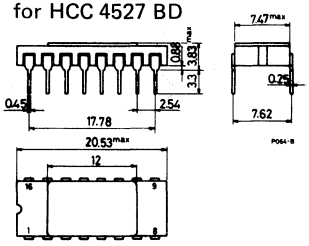
Dual in-line ceramic package for HCC/HCF 4527 BF



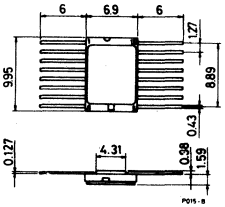
Dual in-line plastic package for HCF 4527 BE



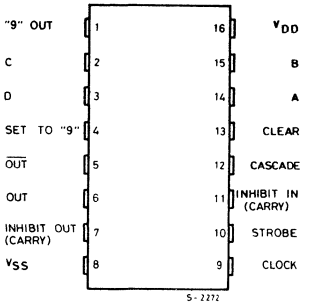
Dual in-line ceramic package for HCC 4527 BD



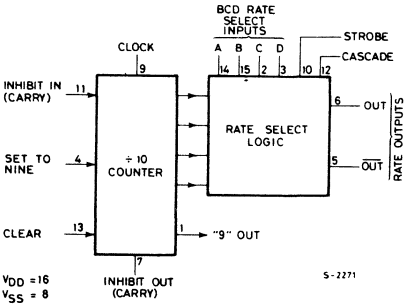
Ceramic flat package for HCC 4527 BK



CONNECTION DIAGRAM



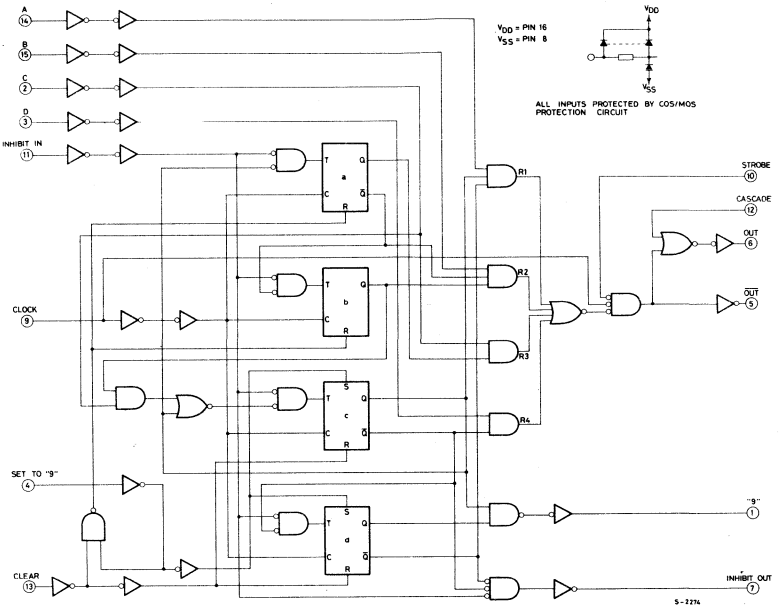
FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM



TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR	SET	OUT	$\overline{OUT}$	INH OUT	"9" OUT
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	▲	▲	H	▲
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	●	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

● Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).
▲ Depends on internal state of counter.

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	V_{DD} (V)	Values Min.	Typ.	Max.	Unit
t_{PHL}, t_{PLH} Propagation delay time	Clock to out		5		110	220	
			10		55	110	ns
			15		45	90	
	Clock or strobe to out		5		150	300	
			10		75	150	ns
			15		60	120	
	Clock to inhibit out high level to low level		5		320	640	
			10		145	290	ns
			15		100	200	
	Low level to high level		5		250	500	
			10		100	200	ns
			15		75	150	
	Clear to out		5		380	760	
			10		175	350	ns
			15		130	260	
	Clock to "9" or "1" out		5		300	600	
			10		125	250	ns
			15		90	180	
	Cascade to out		5		90	180	
			10		45	90	ns
			15		35	70	
	Inhibit input to inhibit out		5		130	260	
			10		60	120	ns
			15		45	90	
	Set to out		5		330	660	
			10		150	300	ns
			15		110	220	
t_{THL}, t_{TLH} Transition time			5		100	200	
			10		50	100	ns
			15		40	80	
f_{CL} Maximum clock frequency			5	1.2	2.4		
			10	2.5	5		MHz
			15	3.5	7		
t_W Clock pulse width			5	330	165		
			10	170	85		ns
			15	100	50		
t_r, t_f Clock rise or fall time			5			15	
			10			15	μs
			15			15	
t_W Set or clear pulse width			5	160	80		
			10	90	45		ns
			15	60	30		

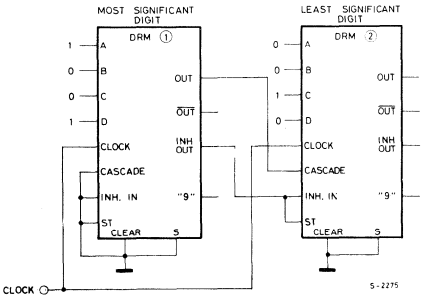
DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

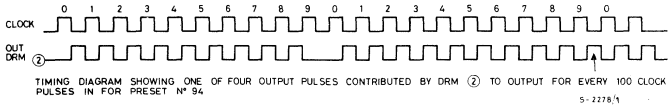
Parameter		Test conditions	Values			Unit
			V_{DD} (V)	Min.	Typ.	Max.	
t_{setup}	Inhibit input setup time		5	100	50		ns
			10	40	20		
			15	20	10		
t_R	Inhibit input removal time		5	240	120		ns
			10	130	65		
			15	110	55		
t_R	Set removal time		5	150	75		ns
			10	80	40		
			15	50	25		
t_R	Clear removal time		5	60	30		ns
			10	40	20		
			15	30	15		

APPLICATIONS NOTE

For fractional multipliers with more than one digit, **HCC/HCF 4527** devices may be cascaded in two different modes: the Add mode and the Multiply mode. See figs. 1 and 3.

Fig. 1 - Two **HCC/HCF 4527B** cascaded in the "Add" mode with a preset number





When two units are cascaded in Add mode and programmed to 9 and 4 respectively, the more significant unit will have 9 output pulses for every 10 input pulses and the other unit will have 4 output pulses for every 100 input pulses for a total of $\frac{9}{10} + \frac{4}{100} = \frac{94}{100}$.

APPLICATIONS NOTE (continued)

The Addition of two variables, A and B is instead obtained with this application:

Fig. 2 - Addition of two variables, A and B

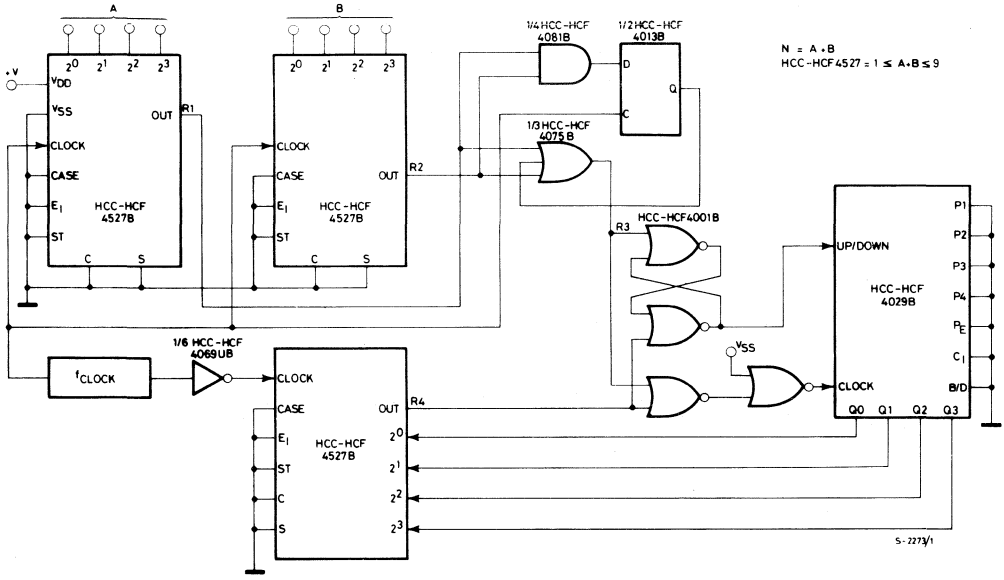
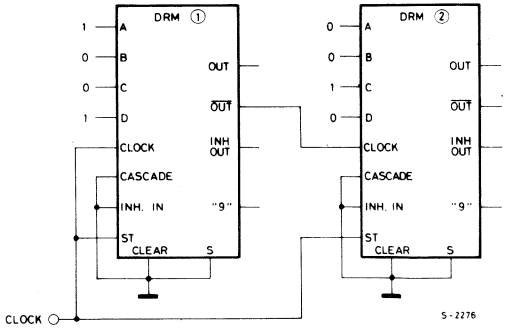


Fig. 3 - Two **HCC/HCF 4527B** cascaded in the "Multiply" mode with a preset number



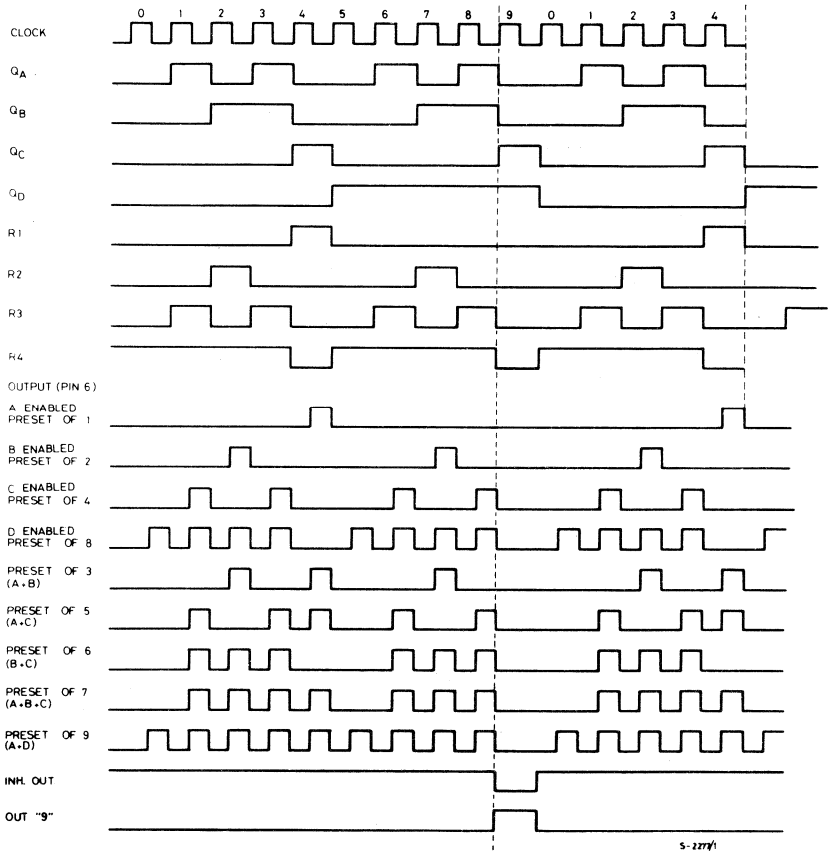
In the Multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one: I_f $N_1 = 9$ and $N_2 = 4$

$f_{out2} = (\frac{4}{10}) \cdot f_{out1}$ $\quad f_{out1} = \frac{9}{10} f_{clock}$ $\quad f_{out2} = \frac{4}{10} \times (\frac{9}{10} f_{clock}) = \frac{36}{100} f_{clock}$

There fore 36 output pulses for every 100 clock input pulses.

APPLICATIONS NOTE (continued)

Fig. 4 - Timing diagram (see Logic Diagram)



COS/MOS INTEGRATED CIRCUIT

PRELIMINARY DATA

8-BIT PRIORITY ENCODER

- CONVERTS FROM 1 OF 8 TO BINARY
- PROVIDES CASCADING FEATURE TO HANDLE ANY NUMBER OF INPUTS
- GROUP SELECT INDICATES ONE OR MORE PRIORITY INPUTS
- QUIESCENT CURRENT SPECIFIED TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4532B** (extended temperature range) and **HCF 4532B** (intermediate temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4532** consists of combinational logic that encodes the highest priority input (D7-D0) to a 3-bit binary code. The eight inputs, D7 through D0, each have an assigned priority. D7 is the highest priority and D0 is the lowest. The priority encoder is inhibited when the chip-enable input E_I is low. When E_I is high, the binary representation of the highest-priority input appears on output lines Q2-Q0, and the group select line GS is high to indicate that priority inputs are present. The enable-out (E_O) is high when no priority inputs are present. If any one input is high, E_O is low and all cascaded lower-order stages are disabled.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

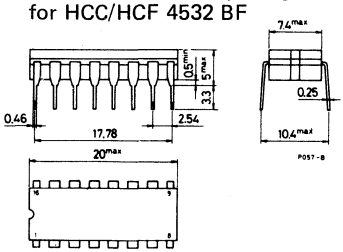
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

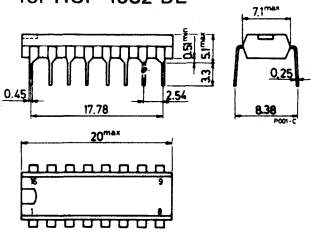
HCC 4532 BD for dual in-line ceramic package
HCC 4532 BF for dual in-line ceramic package, frit seal
HCC 4532 BK for ceramic flat package
HCF 4532 BE for dual in-line plastic package
HCF 4532 BF for dual in-line ceramic package, frit seal

MECHANICAL DATA (dimensions in mm)

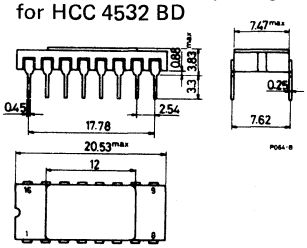
Dual in-line ceramic package
for HCC/HCF 4532 BF



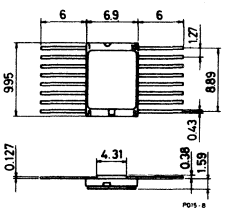
Dual in-line plastic package
for HCF 4532 BE



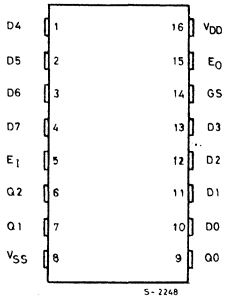
Dual in-line ceramic package
for HCC 4532 BD



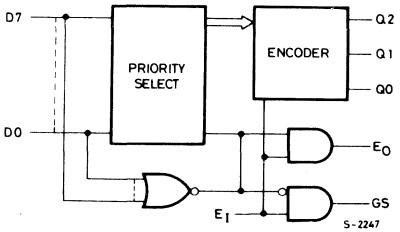
Ceramic flat package
for HCC 4532 BK



CONNECTION DIAGRAM



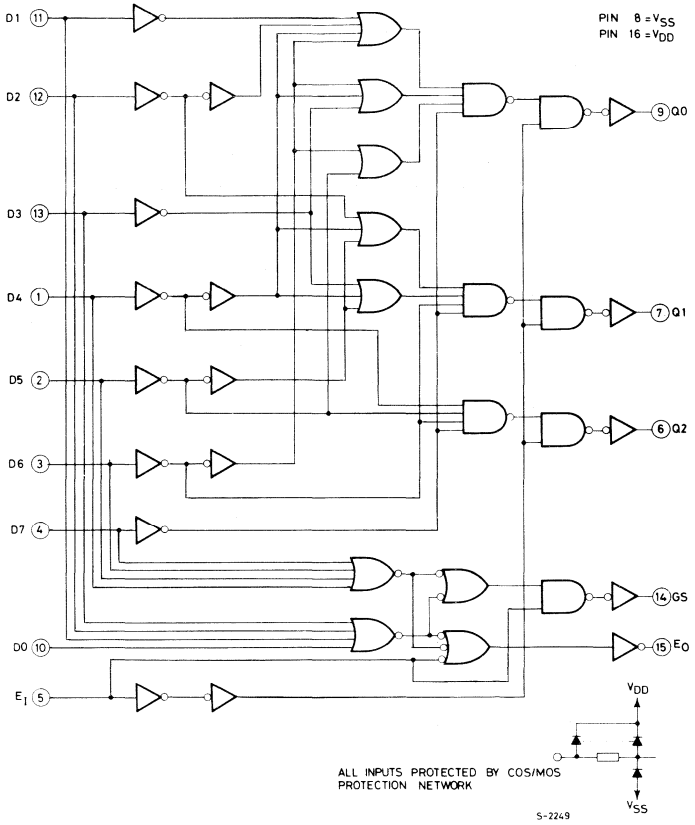
FUNCTIONAL DIAGRAM



RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

LOGIC DIAGRAM



TRUTH TABLE

Input									Output				
E_I	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_O
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1 ≡ High Logic 0 ≡ Low

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current		0/18			18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
C_i**	Input capacitance									5	7.5			pF

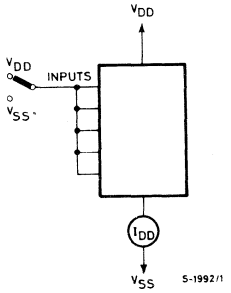
* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

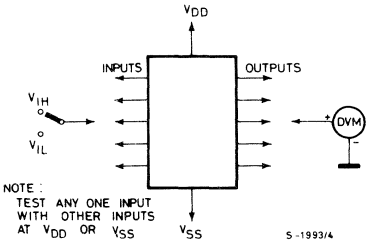
Parameter	Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time (E_I to E_O, E_I to GS)		5		110	220	ns
		10		55	110	
		15		45	85	
t_{PLH}, t_{PHL} Propagation delay time (E_I to Qm, Dn to GS)		5		170	340	ns
		10		85	170	
		15		65	125	
t_{PLH}, t_{PHL} Propagation delay time (Dn to Q_M)		5		220	440	ns
		10		110	220	
		15		85	160	
t_{TLH}, t_{THL} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	

TEST CIRCUITS

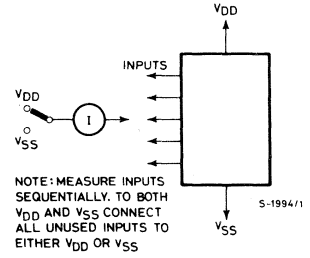
Input leakage current



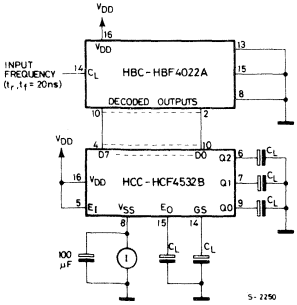
Noise immunity



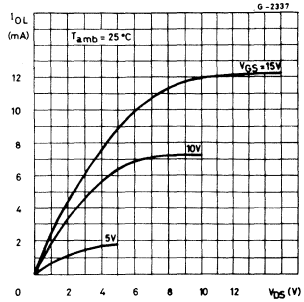
Quiescent device current



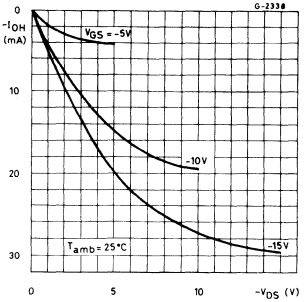
Dynamic power dissipation



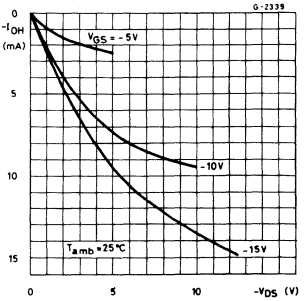
Minimum output low (sink) current characteristics



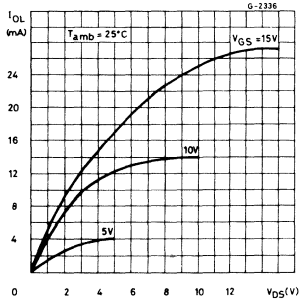
Typical output high (source) current characteristics



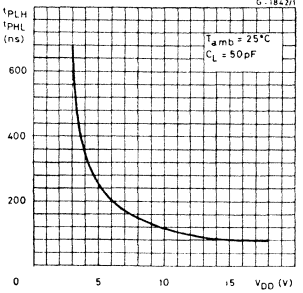
Minimum output high (source current characteristics



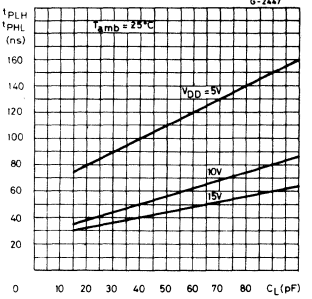
Typical output low (sink) current characteristics



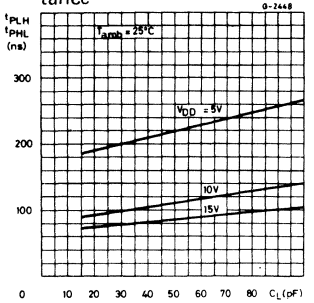
Typical propagation delay (Dn to Qm) vs. supply voltage



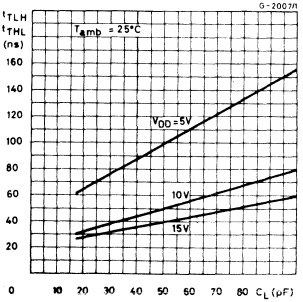
Typical propagation delay (E_I to GS, E_I to E_O) vs. load capacitance



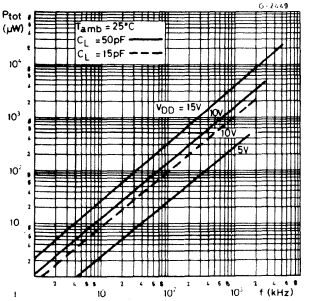
Typical propagation delay (Dn to Qm) vs. load capacitance



Typical transition time vs. load capacitance

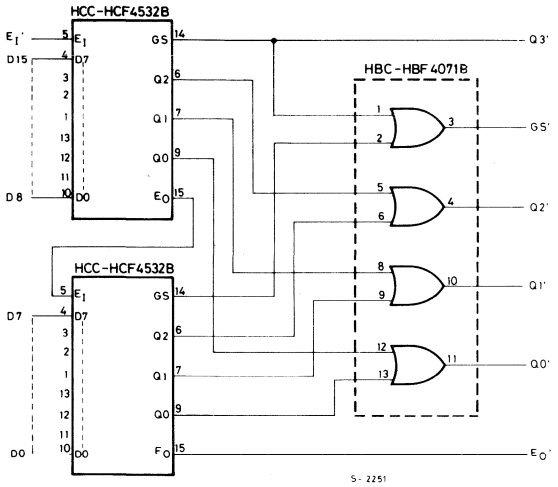


Typical dynamic power dissipation vs. frequency

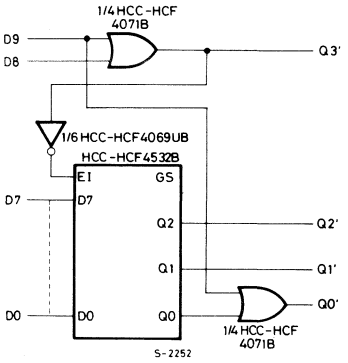


APPLICATIONS

16-level priority encoder



0-to-9 keyboard encoder



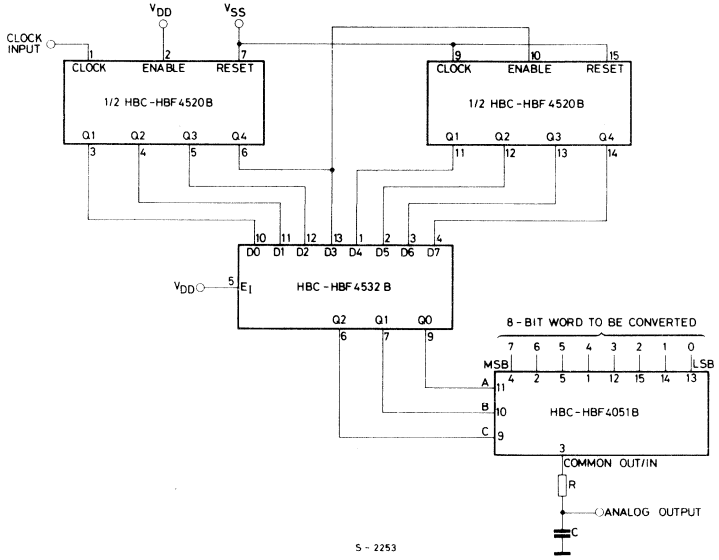
TRUTH TABLE

Input										Output				
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q3'	Q2'	Q1'	Q0'
1	X	X	X	X	X	X	X	X	X	0	1	0	0	1
0	1	X	X	X	X	X	X	X	X	0	1	0	0	0
0	0	1	X	X	X	X	X	X	X	1	0	1	1	1
0	0	0	1	X	X	X	X	X	X	1	0	1	1	0
0	0	0	0	1	X	X	X	X	X	1	0	1	0	1
0	0	0	0	0	1	X	X	X	X	1	0	1	0	0
0	0	0	0	0	0	1	X	X	X	1	0	0	1	1
0	0	0	0	0	0	0	1	X	X	1	0	0	1	0
0	0	0	0	0	0	0	0	1	X	1	0	0	0	1
0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care Logic 1 ≡ High Logic 0 ≡ Low

APPLICATIONS (continued)

DIGITAL TO ANALOG CONVERSION



HCC/HCF 4555B
HCC/HCF 4556B

PRELIMINARY DATA

DUAL BINARY TO 1 OF 4 DECODER/DEMULTIPLEXERS:
4555B OUTPUTS HIGH ON SELECT
4556B OUTPUTS LOW ON SELECT

- EXPANDABLE WITH MULTIPLE PACKAGES
- STANDARD, SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE-TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4555B**, **HCC 4556B** (extended temperature range) and the **HCF 4555B**, **HCF 4556B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.
The **HCC/HCF 4555B** and **HCC/HCF 4556B** are dual one-of-four decoders/demultiplexers. Each decoder has two select inputs (A and B), an Enable input ($\overline{E}$), and four mutually exclusive outputs. On the **HCC/HCF 4555B** the outputs are high on select; on the **HCC/HCF 4556B** the outputs are low on select. When the Enable input is high, the outputs of the **HCC/HCF 4555B** remain low and the outputs of the **HCC/HCF 4556B** remain high regardless of the state of the select inputs A and B.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

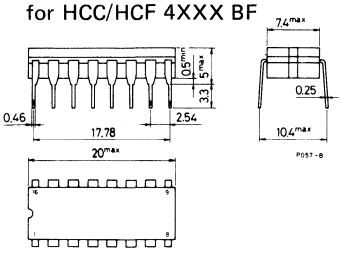
ORDERING NUMBERS:

HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

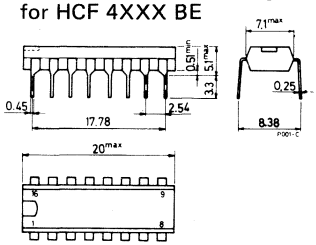
HCC/HCF 4555B
HCC/HCF 4556B

MECHANICAL DATA (dimensions in mm)

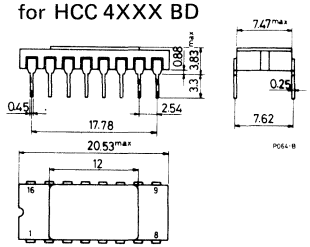
Dual in-line ceramic package
for HCC/HCF 4XXX BF



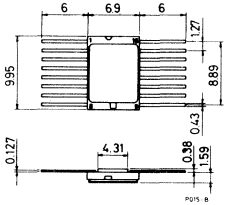
Dual in-line plastic package
for HCF 4XXX BE



Dual in-line ceramic package
for HCC 4XXX BD

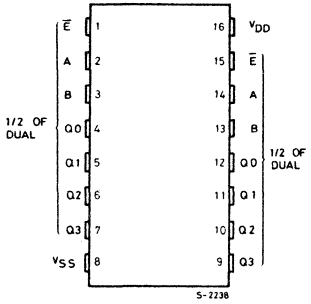


Ceramic flat package
for HCC 4XXX BK

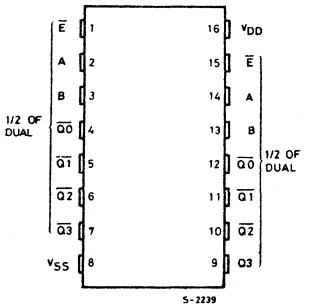


CONNECTION DIAGRAMS

For **4555B**



For **4556B**

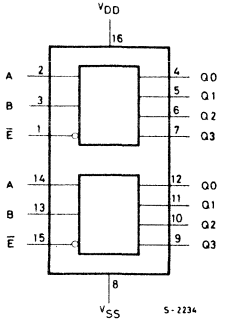


RECOMMENDED OPERATING CONDITIONS

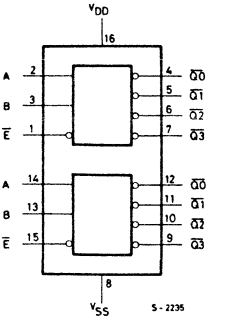
V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

FUNCTIONAL DIAGRAMS

For **4555B**

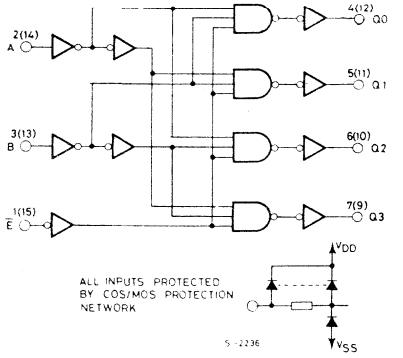


For **4556B**

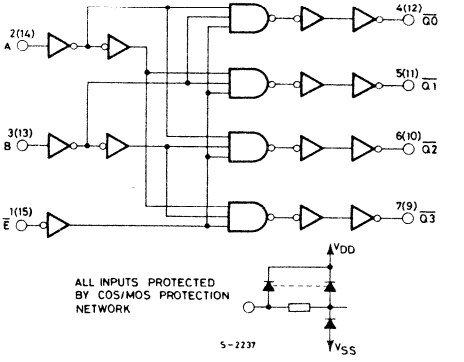


LOGIC DIAGRAMS

For **4555B**



For **4556B**



TRUTH TABLE

INPUTS ENABLE SELECT			OUTPUTS 4555B				OUTPUTS 4556B			
Ē	B	A	Q3	Q2	Q1	Q0	Q̄3	Q̄2	Q̄1	Q̄0
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = DON'T CARE

LOGIC 1 ≡ HIGH
LOGIC 0 ≡ LOW

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

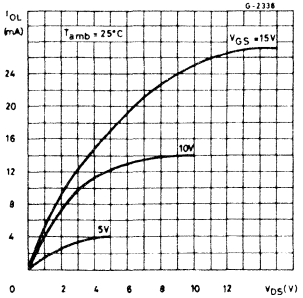
Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent supply current		0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
			0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
			0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
			0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
			0/10	0.5		10	1.5		1.3	2.6		1.1		
			0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH},I_{IL}**	Input leakage current		0/18			18		±0.1		±10^{-5}	±0.1		± 1	μA
C_I**	Input capacitance									5	7.5			pF

* T_{Low} = - 55°C for **HCC** device; - 40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device; + 85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V
** Any input

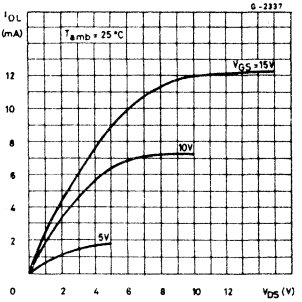
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} values is 0,3%/°C, all input rise and fall times = 20 ns)

Parameter	Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL} Propagation delay time (A or B input to Any Output)		5		220	440	ns
		10		95	190	
		15		70	140	
t_{PLH}, t_{PHL} Propagation delay time ($\overline{E}$ input to Any Output)		5		200	400	ns
		10		85	170	
		15		65	130	
t_{TLH}, t_{THL} Transition time		5		100	200	ns
		10		50	100	
		15		40	80	

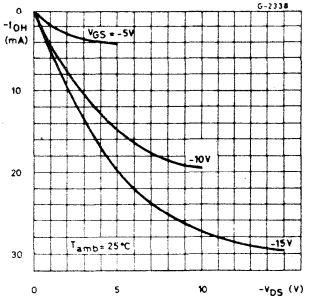
Typical output low (sink) current characteristics



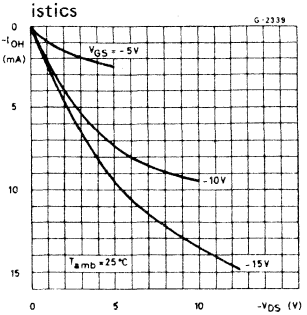
Minimum output low (sink) current characteristics



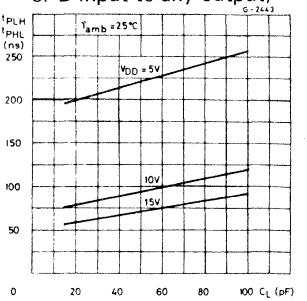
Typical output high (source) current characteristics



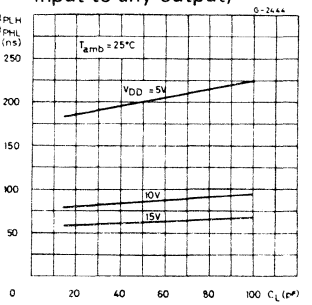
Minimum output high (source) current characteristics



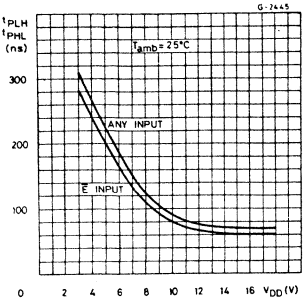
Typical propagation delay time vs. load capacitance (A or B input to any output)



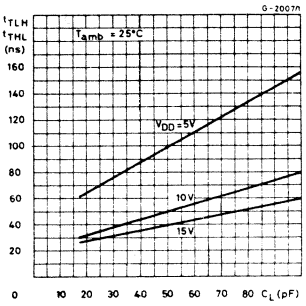
Typical propagation delay time vs. load capacitance ($\overline{E}$ input to any output)



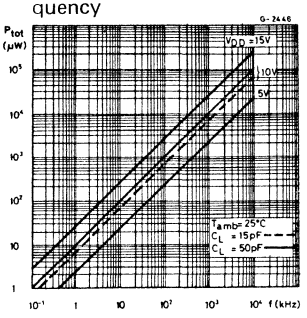
Typical propagation delay time vs. supply voltage



Typical transition time vs. load capacitance

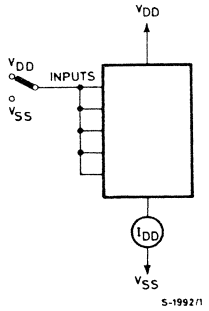


Typical dynamic power dissipation/per device vs. frequency

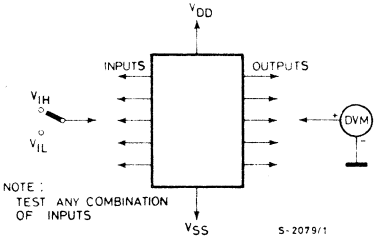


TEST CIRCUITS

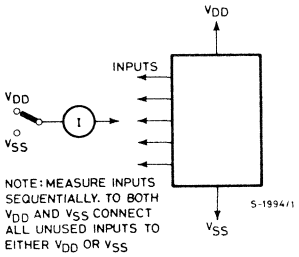
Quiescent device current



Noise immunity

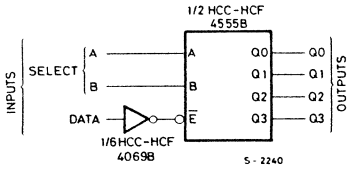


Input leakage current



APPLICATIONS

1 of 4 line data demultiplexer using HCC/HCF 4555B

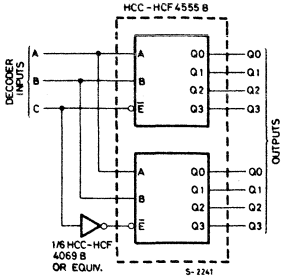


Truth table

SELECT INPUTS		OUTPUTS			
B	A	Q0	Q1	Q2	Q3
0	0	DATA	0	0	0
0	1	0	DATA	0	0
1	0	0	0	DATA	0
1	1	0	0	0	DATA

APPLICATIONS (continued)

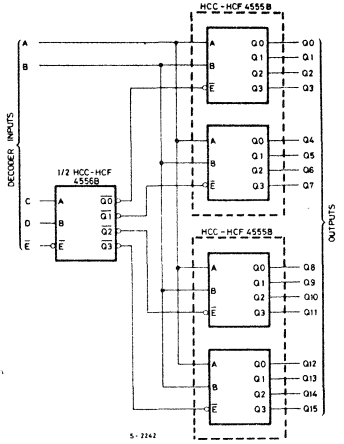
1 of 8 decoder using HCC/HCF 4555B



Truth table

INPUTS			Q OUTPUTS							
C	B	A	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

1 of 16 decoder using HCC/HCF 4555B and HCC/HCF 4556B

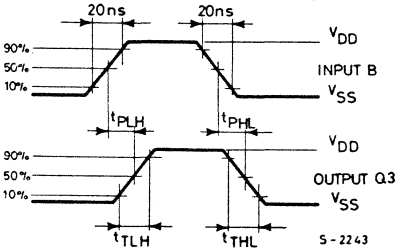


Truth table

INPUTS					Q OUTPUTS														
E	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

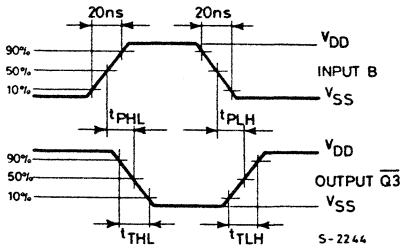
X = don't care

HCC/HCF 4555B input to Q3 output dynamic signal waveforms



f_I = 1MHz, 50% DUTY CYCLE

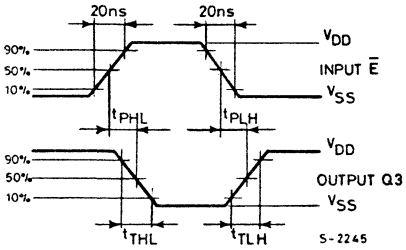
HCC/HCF 4556B input to $\overline{Q3}$ output dynamic signal waveforms



f_I = 1MHz, 50% DUTY CYCLE

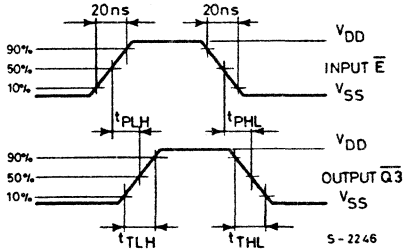
APPLICATIONS (continued)

HCC/HCF 4555B $\overline{E}$ input to Q3 output dynamic signal waveforms



f_I = 1MHz, 50% DUTY CYCLE

HCC/HCF 4556B $\overline{E}$ input to $\overline{Q3}$ output dynamic signal waveforms



f_I = 1MHz, 50% DUTY CYCLE

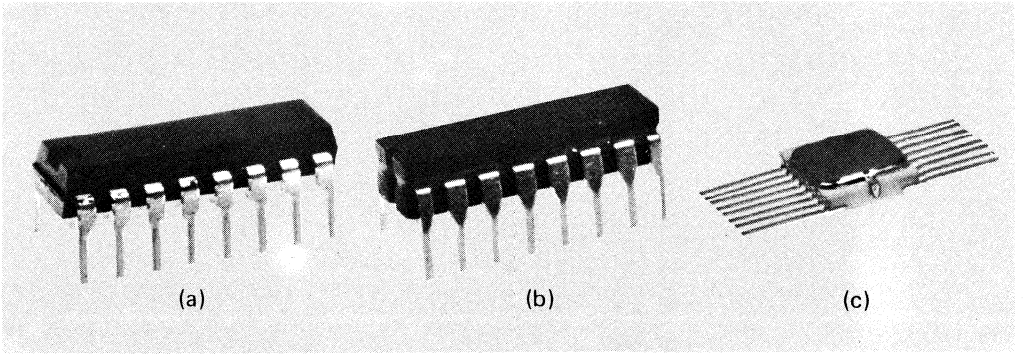
RELIABILITY REPORT

RESULTS OF THE RELIABILITY STUDIES AND OF THE IMPROVEMENTS MADE BY SGS-ATES TO ITS COS/MOS FAMILY

INTRODUCTION

The HB 4000 series of COS-MOS integrated circuits is a logic family of devices using P-channel and N-channel complementary MOS technology; since appearing in 1968, the family has achieved much success in consumer, industrial, military and space applications.
SGS-ATES started C-MOS (Complementary Metal Oxide Semiconductor) production in 1973 and now produces more than 100 standard types from the A and B families; these are mounted in both plastic and ceramic packages (Fig. 1).

Fig. 1 - C-MOS packages: a) Dual in-line plastic
b) Dual in-line ceramic
c) Ceramic flat-pack



In 1976, the devices of SGS-ATES C-MOS range become the first of their type to be approved by the European Space Agency (ESA); this followed a three-year evaluation-qualification programme which was carried out under the supervision of the European Space Technology Center (ESTEC). See also [1].

C-MOS CHARACTERISTICS

The main advantages offered by C-MOS devices with respect to corresponding bipolar devices (DTL, LPS, TTL, ECL, HLL) are:

a) Very low power dissipation (typically 10 nW/gate; 10 μW/MSI)
b) wide voltage range (3 to 18V)
c) high input impedance (typically $10^{12}\,\Omega$)
d) high noise immunity (typically 45% of supply voltage)

On the other hand, due to their high sensitivity to electrostatic discharge, C-MOS devices require greater care in handling and have a slower switching speed than certain bipolar IC families.
Table 1 shows the typical gate propagation times for C-MOS and for the other logic families.

Table I

Family	ECL	LPS	TTL	DTL	HLL	C-MOS
Propagation Time (ns)	2	5	10	30	110	35

From the consideration shown above, it can be seen that C-MOS can be used with advantage in all applications where high speed is not of fundamental importance.

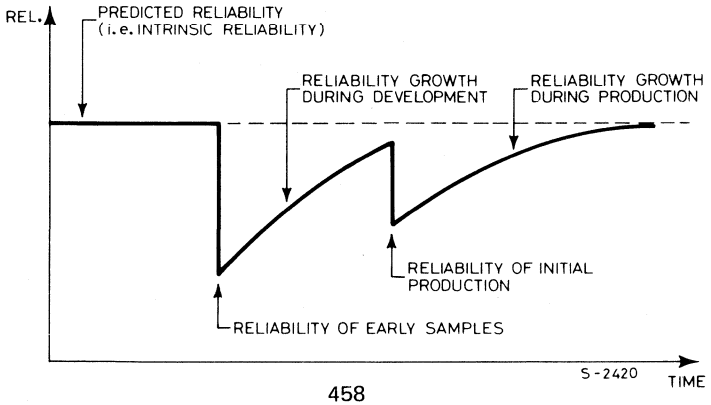
C-MOS RELIABILITY

It can now be said with confidence that the intrinsic reliability of C-MOS devices is equal to or better than that of the other logic families, for the following reasons:

a) greater simplicity of fabrication (fewer operations)
b) low operating temperature (high long-term reliability)
c) low thermal stress between die and package
d) low current density in aluminium paths (absence of electromigration)

Nevertheless, in the initial production phase, all major manufacturers and users encountered reliability problems; these problems could, on the one hand, be attributed to handling (electrostatic discharges and field failure due to overvoltages) and, on the other, to the fact that, unlike bipolar technology, complementary MOS technology was new and consequently the peak of the learning curve had not been reached (Fig. 2).

Fig. 2 - Learning curve during the development and production phases



The intrinsic reliability level of the technology having been ascertained through ESA homologation and accelerated laboratory tests, SGS-ATES took four principal actions to achieve this level through the identification and elimination of defects:

- intensive analysis of rejects from internal tests, from customer tests and from the field; the latter case involved close cooperation with the equipment manufacturers. Tests and failure analysis were also effected on competitors' devices;
- transfer of information concerning failure mechanisms to project and product managers;
- corrective actions by design and production engineering staff to eliminate the cause of failure or to improve device ruggedness;
- introduction or intensification of quality and reliability tests to maintain the process under control.

The main improvements introduced to C-MOS devices during the learning period relate to masking, passivation and electrical testing, in particular:

- layout of components in the integrated circuit
- phosphorous content in P-Vapox
- oxide contamination
- gate oxide thickness
- hermeticity of ceramic and plastic package
- metallization.

These improvements were achieved by means of the following actions:

- redesign of certain masks
- tighter control on the percentage of phosphorous in the P-Vapox
- oxide gettering and improved environmental conditions to eliminate process impurities
- electrical stress testing of gate oxide
- introduction of new resin (epoxy B) for plastic packages and new sealing glass for ceramic packages
- modifications to the design of the oxide steps and inspection under Scanning Electron Microscope.

CONCLUSIONS

The intrinsic reliability of C-MOS technology has been reached by SGS-ATES products as a result of an intense testing and verification programme and a through understanding of the characteristic failure mechanisms.
We can now say that the reliability of C-MOS devices is equal to that of bipolar logic devices. In particular, the use of new plastics and new sealing glasses, have resulted in highly hermetic packages; this is a fundamental requirement of C-MOS devices since they are sensitive to adverse environmental conditions, especially moisture.
For plastic devices, the number of rejects in temperature-humidity-bias testing (85°C, 85% R.H., with biasing) has been reduced by a factor of ten following the introduction of the new resin which has raised the wearout limit by a factor of four.
On the basis of long-term test data, failure rates of the order of 10^{-6} failures/hour (at V_{DD}= 15V; T_{amb}= 85°C for plastic, T_{amb}= 125°C for ceramic) have been established with a confidence level of 60%; this represents a failure rate of 10 to 200 FIT (*) under normal operating conditions (55°C).

(*) FIT: Failure in time = (failures/hour) x 10^{-9}.
= (%/1000 hour) x 10^{-4}

PACKAGE RELIABILITY

Apart from physically supporting the active element (the die), the main function of the package is to protect it from harmful environmental agents, especially humidity.
Until a few years ago hermetically sealed packages of metal or ceramic were used; more recently plastic packaging has become popular for high volume production, largely for reasons of cost.

A-PLASTIC PACKAGE

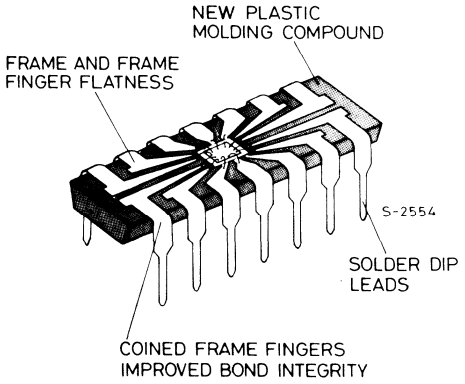
The plastic package for C-MOS circuits (figure 3) consists of:

- a KOVAR (Fe 54%, Ni 29%, Co 17%) or ALLOY 42 (Fe 58%, Ni 42%) frame
- gold interconnecting wires (1 mil)
- type B epoxy encapsulating resin (Novolac)

The resin used at SGS-ATES has optimum characteristics:

- strict control of contaminants ($< 10^{11}$ of Na^+, K^+, Cl^- ions per cm^2) capable of modifying device electrical characteristics and promoting metal corrosion;
- excellent adherence to frame metal, preventing moisture from entering at the resin-metal interface;
- optimum shrinkage (5 to 7%) during polymerization so as to keep wires under pressure even at maximum operating temperature (150°C); the glass transition temperature, above which the expansion coefficient rises significantly, is greater than 165°C;
- resistance to such harmful environments as salt atmosphere or industrial fumes;
- high chemico-physical stability versus time;
- non flammability.

Fig. 3 - C-MOS plastic package



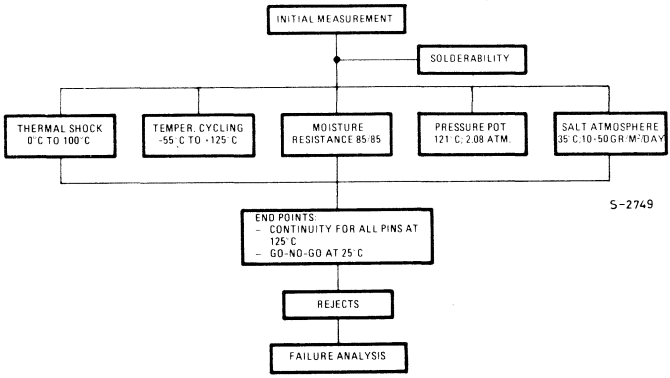
1A - EVALUATION OF PLASTIC PACKAGE RELIABILITY

To evaluate the reliability parameters of plastic package for C-MOS devices a series of tests (figure 4) is carried out to determine package behaviour in terms of:

- resistance to moisture
- resistance to temperature excursions.

N.B.: The plastic package, which represents a compact structure with the interconnecting wires rigidly encapsulated, is particularly resistant to mechanical stresses, such as shock, acceleration and vibration. Most of the mechanical tests carried out to evaluate the reliability of hermetic packages are not relevant, therefore, to plastic packages.

Fig. 4 - Reliability test programme for C-MOS plastic package

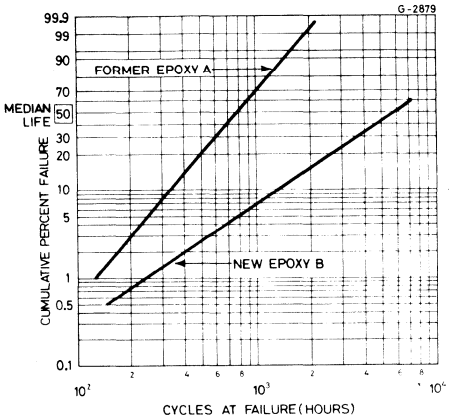


a) **Temperature cycling**

Thermal shock (liquid to liquid) and temperature cycling (air to air) tests at the extremes of operating temperature, check the internal interconnection system for resistance to mechanical stresses. In operation these derive from temperature excursions due to the different expansion coefficients of frame, wires, die and encapsulation.

Typical results of temperature cycling between -55°C and +125°C are given in the WEIBULL probability chart (figure 5).

Fig. 5 - WEIBULL graph with results of thermal cycling tests



b) **Climatic chamber and pressure pot**

These tests are carried out to determine the package's resistance to moisture reaching the die and reacting chemically with the aluminium.

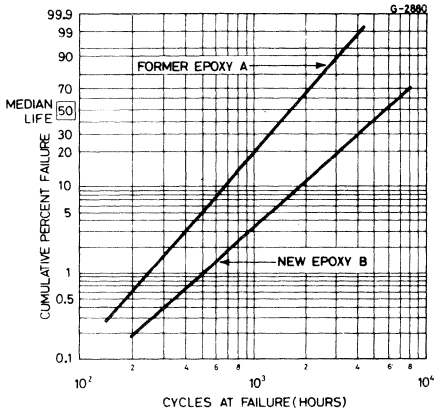
Such chemical reaction is particularly damaging if the moisture contains soluble ionic impurities drawn from the resin during penetration.

The pressure pot test forces moisture into the package through a combination of high temperature and high pressure.

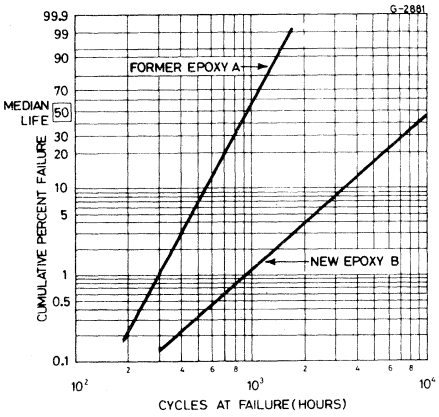
An electrical field externally applied will accelerate aluminium corrosion due to electrolytic conduction between adjacent tracks of different potential.

Figures 6a and 6b give the results obtained in moisture testing with the climatic chamber with biasing, and with the pressure pot.

Fig. 6 - Results of the 85°C/85% RH test with biasing (a) and of the pressure pot test (b)



(a)



(b)

c) **Salt chamber**

The devices are subjected to the action of a saline mist obtained by evaporating a solution of sodium chloride (NaCl).

A substantial presence of salt accelerates aluminium corrosion even without biasing, the sodium penetrating the plastic and directly reaching the inside of the device.

Table II presents the data from internal homologation (*) testing of the C-MOS plastic package; table III gives the results of routine testing of production devices during the period May 1976 to May 1977.

(*) Tests to which a process or a product is subjected before being transferred to production. These tests are usually more severe than routine ones.

Table II
Summary of homologation tests carried out on C-MOS plastic package.

Test	Sample	Duration	Rejects
Thermal Shock -55°C to +125°C (Liquid to Liquid)	50	100 Cycles 200 Cycles 500 Cycles	0 0 1 *
Temperature Cycling -65°C to +150°C	50	100 Cycles 200 Cycles 500 Cycles 1000 Cycles 2000 Cycles	0 0 0 1 ** 3 **
	100	100 Cycles 200 Cycles 500 Cycles 1000 Cycles	0 0 0 0
Moisture Resistance 85°C/85% R.H. at 10V	38	340 hours 670 hours 1000 hours	0 1 *** 2 ***
	38	340 hours 670 hours 1000 hours	0 0 1 ***
Pressure Pot 121°C, 2.08 Atm. Abs.	50	24 hours 48 hours 96 hours 168 hours 240 hours	0 0 0 1 *** 3 ***
	50	24 hours 48 hours 96 hours 168 hours	0 0 0 0
Salt Atmosphere 35°C	50	24 hours 48 hours 96 hours	0 0 1 ***
	50	24 hours 48 hours 96 hours	0 0 0

* Broken Die.
** Open Circuit.
*** Electrical Reject

Table III
Summary of reliability test results for the period May 1976 to May 1977

Test	Test Conditions	Quantity	
		Tested	Rejected
Solderability	230°C ± 5°C, 2 ± 0,5 Sec. in Sn (60) - Pb (40)	525	1
Thermal Shock	100 Cycles, 0°C to +100°C	385	0
Thermal Cycle	100 Cycles, -55°C to +125°C	685	2
Moisture Resistance	100 hours, 85°C, 85% R.H.	435	0
Pressure Pot	48 hours, 121°C, 2,08 Atm..	620	0
Salt Atmosphere	24 hours, 35°C	125	0

B-CERAMIC PACKAGE

The ceramic package for C-MOS circuits (figure 7) consists of:

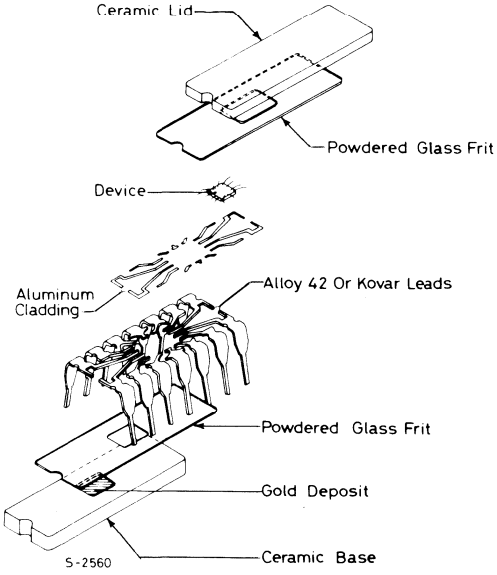
- a KOVAR or ALLOY 42 frame with central area aluminium plated to facilitate soldering of wires to frame pins;
- aluminium interconnecting wires (1 mil);
- ceramic base and cover having a layer of glass with low melting point (450 to 500°C) on one side to ensure hermetic sealing.

1B - CERAMIC PACKAGE RELIABILITY CHARACTERISTICS

The element of greatest importance for the reliability of a ceramic package is the glass seal, which must satisfy two contradictory requirements:

- a melting point low enough not to damage the semiconductor or its mountings (die attach, wire bonding, etc.) during closure.
  The addition of metal oxides (Pb or Zn) lowers the melting point by affecting the purity of the material: this can have a negative effect as far as the second requirement is concerned;
- absence of solid or gaseous impurities which might be set free during the closure heating cycle and invade the internal cavity of the package and hence the die itself.
  Closure is in a dry nitrogen atmosphere to protect the metallization and to ensure that the cavity is filled with an inert gas.

Fig. 7 - Exploded view of C-MOS ceramic package



Another important characteristic of a sealing glass is its ability to withstand thermal stresses without cracking, which would lead to a loss of hermeticity in the package. The main advantages of the ceramic over the plastic package are:

- hermeticity, avoiding metallization corrosion by moisture which has penetrated from the external environment;

– elimination of rejects due to thermal intermittency, since the wires - not being encapsulated - are free to expand and contract within the cavity. Furthermore, defective bonds are more easily detected at electrical testing and can be completely eliminated with appropriate screenings;

– one-type metal interface (Al-Al) of wires and metallization, avoiding fragile cross-metal formations of the "purple plague" type (Au Al 2).

These characteristics, together with the fact that the active element operates in an inert atmosphere, make the ceramic package preferable for applications where:

– long periods of operation life (20 to 40 years) must be assured;
– operation may take place in uncontrolled environments;
– devices are to be screenable, ie, subjected to stresses designed to eliminate the early failure fallout.

On the other hand, the ceramic package is less resistant than the plastic package to mechanical stresses, and thermal stress may affect its hermeticity.

2B - EVALUATION OF CERAMIC PACKAGE RELIABILITY

Reliability testing of the ceramic package is intended particularly to evaluate hermeticity characteristics, including those after severe thermo-mechanical stresses (figure 8).

Fig. 8 - Reliability test programme for C-MOS ceramic package

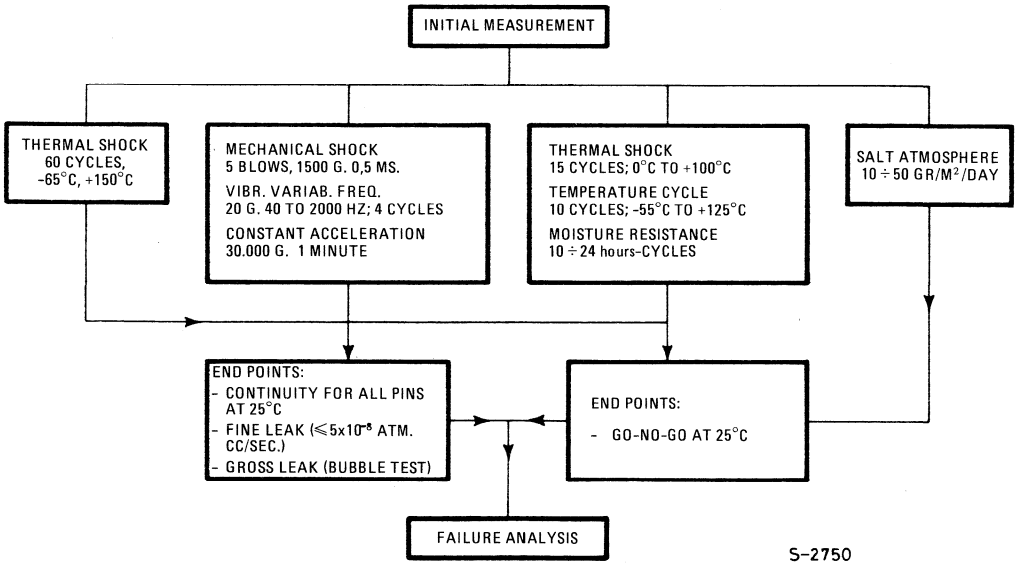


Table IV presents the data from homologation testing of the C-MOS ceramic package; table V gives the results of routine testing of production devices during the period May 1976 to May 1977.

Table IV
Summary of homologation tests carried out on C-MOS ceramic package

Test	Sample	Failures
Thermal Shock, 60 Cycles, -65°C to +150°C	125	0, After Final Leak (5×10^{-8} CC/Sec.) Gross Leak (Bubble Test)
Mechanical Shock, 1500 g., 0,5 MSec., 5 Blows in Each of the 6 Directions. Vibration Variable Frequency 20 g. Peak Acceleration, 40 to 2000 Hz., 4 Times in 3 Directions. Constant Acceleration, 30.000 g., 1 Minute in 3 Directions.	150	0
Thermal Shock, 15 Cycles, 0°C to +100°C Temperature Cycle, 10 Cycles, -55°C to +125°C Moisture Resistance, 240 hours, (10 - 24 hour Cycles)	100	0
Salt Atmosphere, 24 hours, 35°C	95	0

Table V
Summary of reliability test results for the C-MOS ceramic package for the period May 1976 to May 1977.

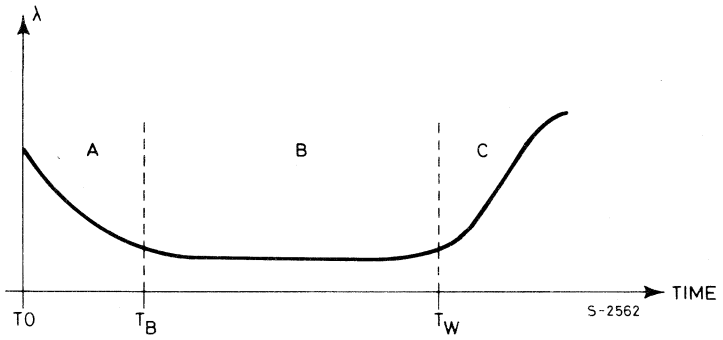
Test	Test Conditions	Quantity	
		Tested	Rejected
Solderability	230°C ± 5°C, 2 ± 0,5 Sec., In Sn (60) - Pb (40)	575	1
Mechanical Shock	1500 g., 0,5 MSec., 5 Blows In Each of the 6 Directions	555	2
Vibration Variable Frequency	20 g., 40 to 2000 Hz., 4 Times In 3 Directions		
Constant Acceleration	20.000 g., 1 Minute In 3 Directions		
Thermal Shock	15 Cycles, 0°C to +100°C	460	1
Temperature Cycle	10 Cycles, -55°C to +125°C		
Moisture Resistance	240 hours (10 - 24 hour Cycles)		
Salt Atmosphere	24 hours 25°C	95	0

LIFE TESTING

Life tests are used to establish experimentally how well C-MOS devices maintain their electrical characteristics in time, and to investigate their failure mechanisms. In these tests the devices are subjected to high temperature storage, or to temperature and voltage stresses (operative life test).
Long term life testing also serves to establish the devices' failure rate (λ): an important design factor for the system manufacturer, bearing both on the performance of this equipment and on the cost of repairs.
The curve of failure rate λ of the components as a function of time is shown in figure 9.

Fig. 9 - This curve is characterized by three phases:

A) Period of infant mortality or initial failures.
B) Period of useful life or random failures.
C) Period of end of life (or wearout).



The failure rate λ curve is not constant for the first hours of operation of semiconductors. It may be wrong to give a single value of λ (the average) in the first 1000 h of life testing because it is not very representative of the two zones: infant mortality and random failures. This section gives the operational λ (random failures zone), while the λ of the initial period is given and analyzed later where the results of the principal screenings applied to C-MOS are examined.

A-HIGH TEMPERATURE STORAGE (150°C)

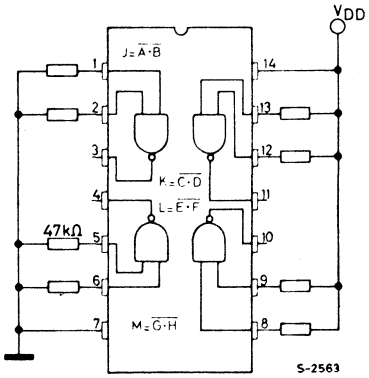
The high temperature storage test serves to investigate temperature-linked failure mechanisms by providing the energy required to trigger certain types of failure due to ion contamination. With plastic packaged devices it is important that the glass transition temperature (approx. 165°C for C-MOS resin) is not exceeded, as otherwise serious mechanical failures, such as breaking of interconnecting wires, can result.
Testing, for both plastic and ceramic packaged C-MOS devices, is for 1000 hours at 150°C.

B-OPERATIVE LIFE TEST

For plastic packaged C-MOS devices the static life test was carried out at a temperature of 85°C and for ceramic packaged devices at 125°C.
Supply voltage was 15V for a duration of 1000 hours.
Initially this testing was carried out on the A series at 10V, but following the redesign of certain masks and the introduction of other improvements previously mentioned, the value was brought progressively to 12V, 13V and the present 15V.
This test is especially useful in revealing die failure mechanisms, particularly those which lead to increased leakage currents and which are usually due to the presence of small quantities of sodium or potassium ions from the fabrication process. These tend to migrate under the effect of the high temperature and the electrical field, to concentrate in certain areas and cause damaging surface inversions.
The test configurations sees half the inputs in the high state, and half in the low, ie: in half, the N-channel MOS inputs conduct and the P are inhibited, and viceversa in the other half.
The outputs are not electrically connected.
Figures 10a and 10b give the static life test diagrams for two typical C-MOS families: gates and shift registers.

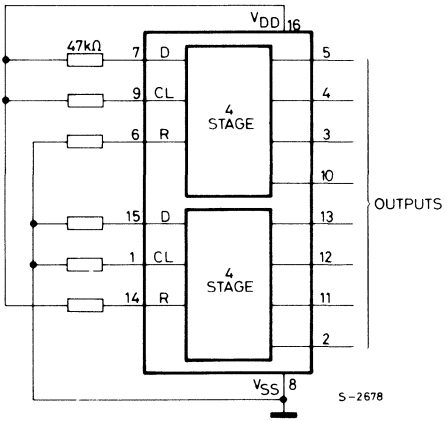
Fig. 10

Nand gate HBC/HBF 4011A



(a)

Shift register HBC/HBF 4015A



(b)

Table VI gives the results of static life and high temperature storage testing for the main C-MOS families.

Table VII and VIII give the failure rates for C-MOS devices in test temperature and in normal operating temperature conditions (55°C), for the two package types.
For the calculation of λ at 55°C, ARRHENIUS' formula was used with an activation energy, $E_A = 1{,}1$ Ev.

Table VI
Summary of results of life test performed on C-MOS devices over the period July 1976 to April 1977.

Device	Operative Life Test (15V)		High Temperature Storage (150°C)	
	Plastic (85°C)	Ceramic (125°C)	Plastic	Ceramic
Gates	66 / 0	270 / 0	45 / 0	210 / 0
Flip-Flops	44 / 1	–	30 / 0	–
Counters	66 / 0	110 / 0	45 / 1	75 / 0
Latches	44 / 0	–	45 / 0	–
Multiplexers	66 / 0	44 / 0	90 / 0	45 / 0
Shift Registers	44 / 0	118 / 2	45 / 0	105 / 1
Arithmetic Circuits	130 / 0	130 / 0	135 / 0	135 / 0
TOTAL	460 / 1	672 / 2	435 / 1	570 / 1

Table VII
Reliability calculation for plastic-packaged C-MOS

Type of Test	Device Hours	Rejects	Failure Rate (λ)	
			Confidence Level 60%	Confidence Level 90%
High Temperature Storage	At 150°C: 287.100 At 55°C: 1.771 550 500	2	0.70% /1000 hours 0.00011%/1000 hours	1.35% /1000 hours 0.00022%/1000 hours
Operative Life Test (Static)	At 85°C: 303.600 At 55°C: 7.899 600	1	0.66% /1000 hours 0.027%/1000 hours	1.28% /1000 hours 0.049%/1000 hours

Table VIII
Reliability calculation for ceramic-packaged C-MOS

Type of Test	Device Hours	Rejects	Failure Rate (λ)	
			Confidence Level 60%	Confidence Level 90%
High Temperature Storage	At 150°C: 376.200 At 55°C: 349.866 000	1	0.54%/1000 hours 0.00058%/1000 hours	1.03%/1000 hours 0.00111%/1000 hours
Operative Life Test (Static)	At 125°C: 443.520 At 55°C: 412.473 600	2	0.71%/1000 hours 0.00076%/1000 hours	1.20%/1000 hours 0.00129%/1000 hours

ELECTRICAL PARAMETERS CHECKED AND END-OF-TEST LIMITS

At suitable time intervals during the life testing (340, 670 and 1000 hours) checks have been made on the variations in certain parameters (reliability parameters), corresponding to characteristic C-MOS failure modes.
Table IX gives the parameters checked and the relative end-of-test limits.

Table IX

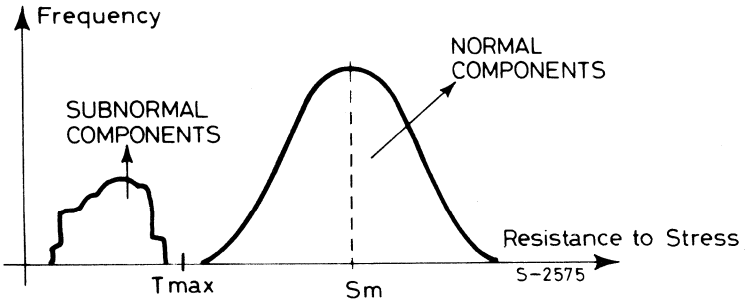
Parameters	End. Of. Test Limits
Functional Test	See Type Truth Table.
Quiescent Current (IL)	+ 100% of Spec. Limit
Input Leakage Current (IIL, IIH)	+ 100% of Spec. Limit
N-Channel MOS Output Current (IDN)	- 10% of Spec. Limit
P-Channel MOS Output Current (IDP)	- 10% of Spec. Limit

THE MOST COMMON SCREENINGS PERFORMED ON C-MOS

1. INTRODUCTION

Components manufacturers are frequently asked to carry out a 100% screening of their products in order to reduce the number of early failures.
Cost considerations are uppermost in a decision of this sort.
System cost will be lowered if the number of components requiring replacement at the assembly or runin phases of the system is itself reduced. On the other hand, components with better than standard initial reliability will be themselves more costly.
The various screenings are intended to eliminate or reduce the higher initial failure rate so that the system failure begins approximately at T_B rather than at To (figure 9).
This type of curve can be accounted for by the fact that a limited number of freak components escape the various checks carried out during and after the fabrication process.
An analysis of component stress resistance result in the curve shown in figure 11.

Fig. 11



With Tmax stress applied, freak components will be destroyed, whereas the resistance of normal components will not be affected.
Many different types of screening can be carried out in practice, and, depending on the cost hazard involved in replacement of the component at system level, a greater or lesser number will be chosen. It is to be borne in mind in this regard that not all screenings are equally effective in removing freak components, which in any event represent the various causes of malfunction in varying proportions.
Apart from more sophisticated applications such as aerospace, common experience has proved the validity of two basic types of screening: electrical burn-in and a sequence of thermal screenings listed below.
Components are 100% electrically selected and accepted by quality control with standard products procedure and at standard products quality levels. They are then subjected 100% to the selected screening and afterwards 100% electrically selected. The lot is finally accepted by quality control with stricter AQL levels than the pre-burn-in acceptance (1). This provides the dual effect of a "screening-double-selection": improvement of reliability with reduction of early failures, and improvement of quality with a lower proportion of pieces out of spec. at the moment of delivery.

2. RESULTS OF SCREENINGS

The above operations involve the rejection not only of the abnormal components destroyed or badly degraded by the screening itself, but also of a certain proportion of pieces close to electrical selection limits. The latter may be rejected because of measuring instrument tolerances or because of small variations in electrical parameters caused by burn-in (2).

(1) See new SGS-ATES SURE programme - 1977 edition.

(2) Large quantity automatic 100% selections may lead to small percentages or fractions of a percent of good pieces being rejected, for many different reasons. These percentages are included in the burn-in rejected figures. An example: contact rejects at sockets of automatic tester.

The second selection eliminates most of the defective pieces (pieces within normal AQL limits) surviving from the first selection. Data sheet limits are used to select the pieces for after burn-in, as they are before the test.
The percentage of rejects during a screening allows calculation of the cost of the screening itself and also provides useful information on product reliability, provided it is used together with reject analysis to determine the main failure mechanisms.
The various failure modes are illustrated and eliminated by means of different types of screening, as shown in the table X. Rejects for degraded electrical parameters alone have been omitted. The percentage, referred to the total number of pieces considered in the failure analysis, of each type of defect is given.
These results are also confirmed by other studies [2].

Table X
Electrical life test or electrical Burn-in

Failure Modes	Failure Causes	Failure Mechanisms	Ceramic	Plastic
Open Short Circuit Leakage Functional Test	Oxides (1)	Short Circuits and Oxide Breakdowns Cracks and Pinholes Inversions and Channeling	39%	33%
Open	Internal Wires (2)	Broken Or Lifted Wires	18%	29%
Open Leakage Short Circuit	Metal	Excess Etch Scratches Foreign Materials Alloy Spikes	15%	12%
Short Circuit Leakage Latch-Up	Masks (3)	Lack of Guard Rings Misalignments	15%	10%
Miscellaneous	Unknown	Not Determined	13%	16%
TOTAL			100%	100%

Table X (continued)
Temperature cycling -65°C to +150°C

Failures Modes	Failure Causes	Failure Mechanisms	Ceramic	Plastic
Open	Internal Wires (2)	Broken or Lifted Wires	13%	43%
Leakage	Package (4)	Lack of Hermeticity	35%	—
Open Short Circuit Leakage	Metal	Excess Etch Scratches Foreign Materials Alloy Spikes	15%	12%
Open Short Circuit Leakage Functional Test	Oxides (1)	Short Circuits and Oxide Breakdowns Cracks and Pinholes Inversions and Channeling	10%	13%
Open Functional Test	Dice	Broken Dice or Defective Die Attach	6%	5%
Leakage Short Circuit Latch-Up	Masks (3)	Lack of Guard Rings Misalignments	5%	5%
Surface Defects	External Leads	Darkening, Low Solderability	4%	4%
Miscellaneous	Unknown	Not Determined	12%	18%
TOTAL			100%	100%

High temperature storage (150°C)

Failures Modes	Failure Causes	Failure Mechanisms	Ceramic	Plastic
Open Short Circuit Leakage Functional Test	Oxides (1)	Short Circuits and Oxide Breakdown	48%	40%
Open	Internal Wires (2)	Broken or Lifted Wires	8%	15%
Open Leakage Short Circuit	Metal	Excess Etch Scratches Foreign Materials Alloy Spikes	15%	10%
Surface Defects	External Leads	Darkening, Low Solderability	10%	10%
Leakage Short Circuit Latch-Up	Masks (3)	Lack of Guard Rings Misalignments	6%	5%
Miscellaneous	Unknown	Not Determined	13%	20%
TOTAL			100%	100%

NOTES: (1) Much reduced since introduction of gate oxide screening.

(2) Wire breakage much reduced since introduction of Epoxy B.

(3) Guard rings have been introduced in the new designs, and these defects have been drastically reduced.

(4) New sealing material for ceramic packages has virtually eliminated hermeticity problems.

Over the last 10 months SGS-ATES has subjected approximately 300,000 C-MOS devices to static burn-in of 168h. An analysis of the results follows.
The mean percentage of C-MOS burn-in rejects is about 5%.
Distribution is not symmetrical among the lots tested, tending to lengthen towards the high percentages (anomalous lots). The median percentage of rejects is below the mean: 3.7%.
These lots with higher reject percentage benefit most from the burn-in test (see figure 12 where yield patterns after burn-in are reported).
Figure 13 shows the curve of functional reject percentages after burn-in (average rejects 1.2%). Functional rejects include catastrophic or non-operative failures.
Figure 14 shows the average yield after burn-in versus the voltage applied during the test. Initially a voltage of 10V was applied to C-MOS devices of A series, but higher voltages have been made necessary by ever increasing applications and reliability requirements. At the same time SGS-ATES introduced, in 1976, the gateoxide stress test, and modified the 100% electrical selection to include much more severe leakage current measurements. The positive effect of these changes is indicated in figure 14 which shows an improvement in yield after burn-in.

Fig. 12 - Yields obtained through normal burn-in (including all types and all voltage applied).

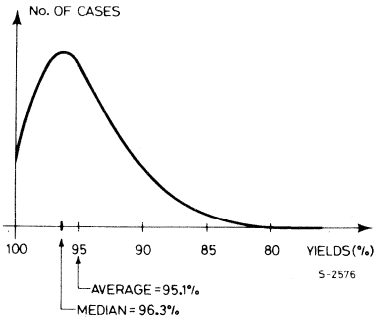


Fig. 13 - Yields obtained with functional test alone.

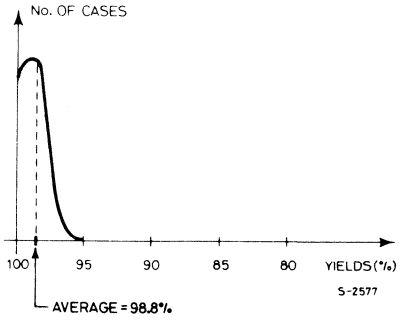
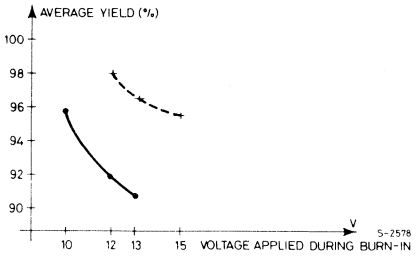


Fig. 14 - Yields curve versus burn-in voltage before the introduction of gate-oxide stress test and new selection criteria.

Yields curve versus burn-in voltage after introduction of gate-oxide stress test and new selection criteria.



Reject percentages in thermal screening (10 temperature cycles +168 h storage at maximum junction temperature) are lower than in the burn-in test, but the lot distribution of rejects is similar to the results in figure 12.
The number of pieces tested in this way is not yet large enough for quantitative conclusions to be drawn such as in figures 12 and 13.

3. EFFECT OF SCREENINGS ON FAILURE RATE

The manufacturer of a given system using C-MOS components must work out what advantage he derives from using screened integrated circuits, an advantage particularly in reduced failure rate in early operation, which should widely repay the extra cost of the components.
The following study of C-MOS devices subjected to electrical burn-in has been carried out, comparing their performance with that of standard pieces, i.e., pieces not subjected to any supplementary screening.
It is to be borne in mind (see paragraph 2) that the failure rate is lower than the burn-in results would indicate, since the majority of pieces rejected by burn-in would in fact function correctly in the user's equipment.
Burn-in conditions being identical to life-test conditions, the following considerations are based on life test results and λ curves.
Going back to figure 11, it is necessary for reliability purposes to distinguish between the freak population of components and the normal population.
It is the latter which defines operation failure rate in systems (i.e., useful life or random failures), a failure rate that is assumed to vary with junction temperature according to Arrhenius' law.
The freak population will define the failure rate for early failures. Rate variation versus junction temperature, as supposed for normal components, can not be taken as valid for this population.
The following considerations are based on the supposition that all freak components are destroyed during early period in systems and that varying proportions of such components can be eliminated by different types of screenings carried out before the components are installed.
The freak population is measured as a percentage of the total number of components and taken as equal to the average percentage of rejects during the first 340 h of electrical life testing. (This hypothesis is confirmed by the average percent of functional burn-in rejects, and by field data).
Information, including customer feedback, also confirms the following hypothesis:

a) 168 h (1 week) of burn-in eliminate from 90 to 95% of early failures [3]. The calculations which follow assume that 95% applies to the more screenable ceramic, and 90% to plastic.

b) Average system ambient temperature is 40 to 60°C. The calculation which follow are based on 55°C.

c) In normal system operating conditions early failures of integrated circuits cease after 2000 to 3000 h. The calculations which follow are based on 3000 h.

d) Variation of λ versus temperature during useful life is calculated with Arrhenius' law and activation energy $E_A = 1.1$ eV.

e) Although the first life and 1000 h storage test measurements were taken at 340 h, it is assumed all the 340 h rejects would already have occurred at 168 h (see point a), above.

The failure rate curve during life test (bathtub curve) may be presented as in figure 15.
Operating life test failure rates have been calculated with 60% on sided confidence level and the reject percentages observed during Operating Life Test (0 to 340 h) and Storage

Test (0 to 340 h) plus temperature cycling have been plotted. With activation energy assumed to be 1.1 eV, λ has been calculated for 340 h to 1000 h at T_{amb}= 55°C.

Fig. 15 - This is considered the steady-state failure rate for C-MOS devices installed in system

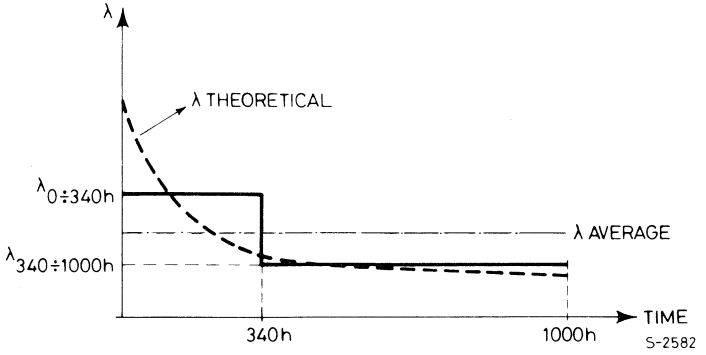


Table XI*

	10 Temperature Cycles + Storage (0 to 340 h) % Observed	Oper. Life Test (0 to 340 h) T_{amb}= 85°C Plastic T_{amb}= 125°C Ceramic; % Observed	Oper. Life Test λ at 60% C.L. T_{amb}= 85°C-Plastic T_{amb}= 125°C-Ceramic		λ At 60% C.L. 340 to 1000 h Calculated With T_{amb}= 55°C
			0 to 340 h	340 to 1000 h	
Plastic	0.61%	0.87%	33.28×10^{-6} h^{-1}	6.66×10^{-6} h^{-1}	2.56×10^{-7} h^{-1}
Ceramic	0.80%	1.19%	40.87×10^{-6} h^{-1}	7.12×10^{-6} h^{-1}	7.66×10^{-9} h^{-1}

* See tables VII and VIII of section 3.

Considering that the reject percentages for the first 340 h of life testing represent the total early failures during 3000 h of system operation, and that, of these, temperature cycling and 340 h storage eliminate only the proportion observed in those tests, we can calculated failure rates for the following three cases:

A) Standard components (no screening).

- In the first 3000 h of system operation

$$\text{Plastic} = \frac{0.87\%}{3000\ \text{h}} = 2.9 \cdot 10^{-6}\,\text{h}^{-1} \qquad \text{(observed)}$$

$$\text{Ceramic} = \frac{1.19\%}{3000\ \text{h}} = 3.96 \cdot 10^{-6}\,\text{h}^{-1} \qquad \text{(observed)}$$

- After 3000 h λ returns to the value found during life tests between 340 and 1000 h, which, referred to ambient temperature T_{amb}= 55°C, gives:

$$\text{Plastic } \lambda = 2.56 \cdot 10^{-7}\,\text{h}^{-1} \qquad \text{(at 60\% C.L.)}$$

$$\text{Ceramic } \lambda = 7.66 \cdot 10^{-9}\,\text{h}^{-1} \qquad \text{(at 60\% C.L.)}$$

B) Components subjected to 10 temperature cycles + 168 h storage.

– In the first 3000 h of system operation

Plastic $\lambda = \frac{(0.87 - 0.61)\%}{3000\ h} = 8.66 \cdot 10^{-7} h^{-1}$ (observed)

Ceramic $\lambda = \frac{(1.19 - 0.80)\%}{3000\ h} = 1.3 \cdot 10^{-6} h^{-1}$ (observed)

– After 3000 h λ returns to the life test 340 to 1000 h λ, giving, at ambient temperature $T_{amb} = 55°C$:

Plastic $\lambda = 2.56 \cdot 10^{-7} h^{-1}$ (at 60% C.L.)

Ceramic $\lambda = 7.66 \cdot 10^{-9} h^{-1}$ (at 60% C.L.)

C) Components subjected to 168 h burn-in.
90% and 95% of potential plastic and ceramic failures, respectively, are eliminated by burn-in.
In the first 3000 h λ will be:

Plastic $\lambda = \frac{0.087\%}{3000\ h} = 2.9 \cdot 10^{-7} h^{-1}$ (observed)

Ceramic $\lambda = \frac{0.0595\%}{3000\ h} = 1.98 \cdot 10^{-7} h^{-1}$ (observed)

– After 3000 h λ returns to the life test 340 to 1000 h λ, giving, at ambient temperature $T_{amb} = 55°C$:

Plastic $\lambda = 2.56 \cdot 10^{-7} h^{-1}$ (at 60% C.L.)

Ceramic $\lambda = 7.66 \cdot 10^{-9} h^{-1}$ (at 60% C.L.)

Ceramic components are more screenable than plastic, and this leads to slightly higher failure rates in ceramic in the early hours of operation, but once the period for early failures has passed (168 h in life test conditions or 3000 h in operating conditions) ceramic shows a better failure performance.
This means that the early failure period for plastic components is probably longer and that we cannot assume exactly the same premises for calculation.
To summarize these results we can now present failure percentages for plastic and ceramic components during the first 3000 h of their installed operation in a system.
Also indicated, for each type of screening, is the reduction factor in number of failures compared with standard components over this same period of time.

Table XII
Evaluation of failure rate in a system (measured in fit)

	FIRST 3000 h			
	Plastic		Ceramic	
	Average Failure Rate	Reduction Factor	Average Failure Rate	Reduction Factor
Standard	3000	–	4000	–
Temp. Cycling + Stor.	860	3.5	1300	3
Burn-In	300	10	200	20
	AFTER FIRST 3000 h			
	250	12	8	500

It is to be borne in mind that the above are average figures.
Referring again to the failure distribution shown in figures 12 and 13, it is worth repeating that screenings are particularly efficient in eliminating those lots whose behaviour is sharply at variance with the average.

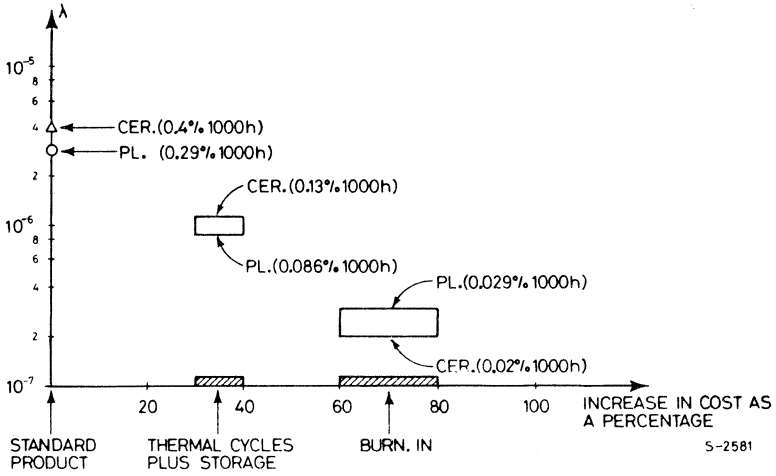
4. INDICATIVE COST OF SOME SCREENINGS

Screening cost depends on several parameters, of which the main are:

- quantity
- supply flow
- specs
- number of kit types and complexity
- time available, i.e., delivery commitments.

There follow some very general indications of how the main types of screening may increase component cost versus standard C-MOS prices.
These increases are read as a function of the expected improvement in failure rates during the first 3000 h of installed operation (figure 16).

Fig. 16 - Average failure rate during the first 3000 h of installed operation, as a function of screenings to which components have been subjected, or to their percentage cost increase relative to cost of standard product.



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[2] RAC, Reliability Workshop, 1976.

[3] J.A. LORANGER, "The case for component burn-in: the gain is well work the price, Electronics, January 23, 1975.

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for use in ESA space programmes, according to ESA/SCC QPL Page 1 Issue 1 Rev – September 77

as recommended by the Space Components Coordination Group.

This certificate is valid until 31rst August 1978

Head of Product Assurance Division | Director Estec | Date

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